Lecturer 6, 7, 8, 9

Radio Communication Systems

Outline

- Introduction
- Types of Digital Modulation
  - Frequency Shift Keying FSK
    - MSK Minimum Shift Keying
  - Amplitude Shift Keying ASK
  - Phase Shift Keying PSK
- M-ary PSK Encoding
  - Quadrature QPSK
  - 8-PSK
- QAM: (8-QAM)
- Carrier Recovery Circuits

Digital Radio

- **Why Digital ?**
  - Ease of processing,
  - Ease of multiplexing, and
  - Noise immunity.
- **All Digital Communications**
  - Transmission, reception and processing of information.
- **Increasing of Information Capacity**
  - No of independent symbols that can be carried through system in a given time.

Information Capacity

- **1928 Hartley introduces useful rule:**
  - Capacity C is proportional to both the bandwidth B and the time T :

$$C \sim B\,T$$

- **1948 Shannon published a limit for C :**

$$C \le B\log_2\left(1+\frac{S}{N}\right) = 3.32\,B\log_{10}\left(1+\frac{S}{N}\right)$$

- $S/N = 1000\ (30\ \mathrm{dB}),\ B = 2.7\mathrm{kHz},\ C$:

$$C \le 2700\log_2(1+1000) \le 26.9\ kbps$$

Limit Misunderstood

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- Above example may be true, but it cannot be done with a binary system.
- To achieve 26.9 kbps through 2.7 kHz channel, each symbol must contain more than one bit of information.
- So, to achieve Shannon limit, digital transmission systems that have more than two output conditions (symbols) must be used.

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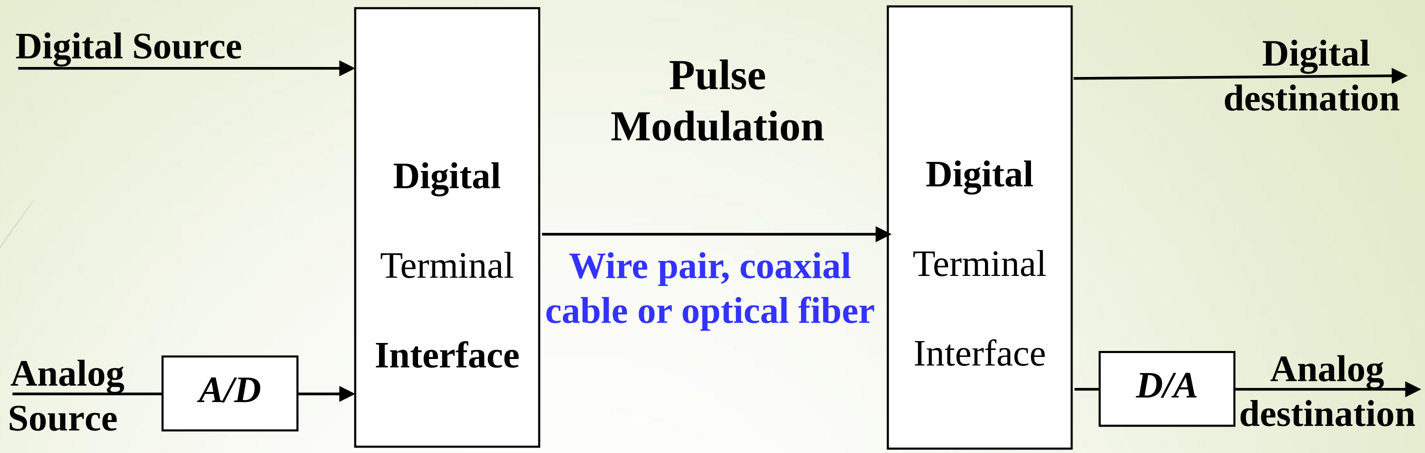
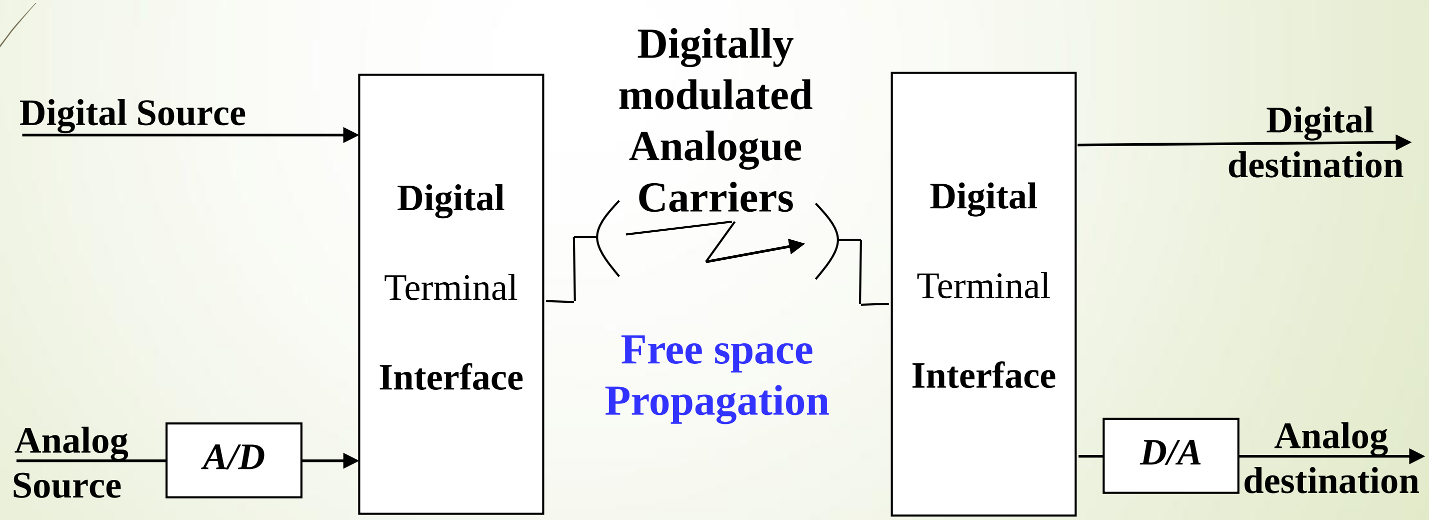


(a) Baseband Transmission



(b) Digital Radio Transmission

Types of Modulation

- تعديل إزاحة السعة Amplitude Shift Keying ASK.
- تعديل إزاحة التردد Frequency Shift Keying FSK.
  - تعديل الإزاحة الدنيا Minimum Shift Keying MSK
  - تعديل الإزاحة الدنيا الجاوسي Gaussian Minimum Shift Keying GMSK.
- تعديل إزاحة الطور Phase Shift Keying PSK.
  - تعديل إزاحة الطور الثنائي Binary Phase Shift Keying BPSK.
  - تعديل إزاحة الطور التفاضلي Differential Phase Shift Keying DPSK.
- تعديل إزاحة الطور متعدد المستويات M-ary Phase Shift Keying.
  - تعديل إزاحة الطور التعامدي Quadrature Phase Shift Keying QPSK.
  - تعديل إزاحة الطور الثماني Eight Levels Phase Shift Keying 8PSK
- تعديل السعة التعامدي Quadrature Amplitude Modulation QAM.

FSK

Frequency Shift Keying

FSK Transmitter Signal

- Simple, low performance.
- Constant envelope angle modulation.

$$v_{FSK}(t) = V_c cos\left[\left(\omega_c + f_m(t)\frac{\Delta\omega}{2}\right)t\right]$$

- $f_m(t)$ binary digital modulating signal
- V_c, ω_c, carrier amplitude, frequency
- Carrier frequency shifts between $\omega_c \pm \Delta\omega/2$
- Shift rate equals the input bit rate f_b b/s.

FSK Transmitter

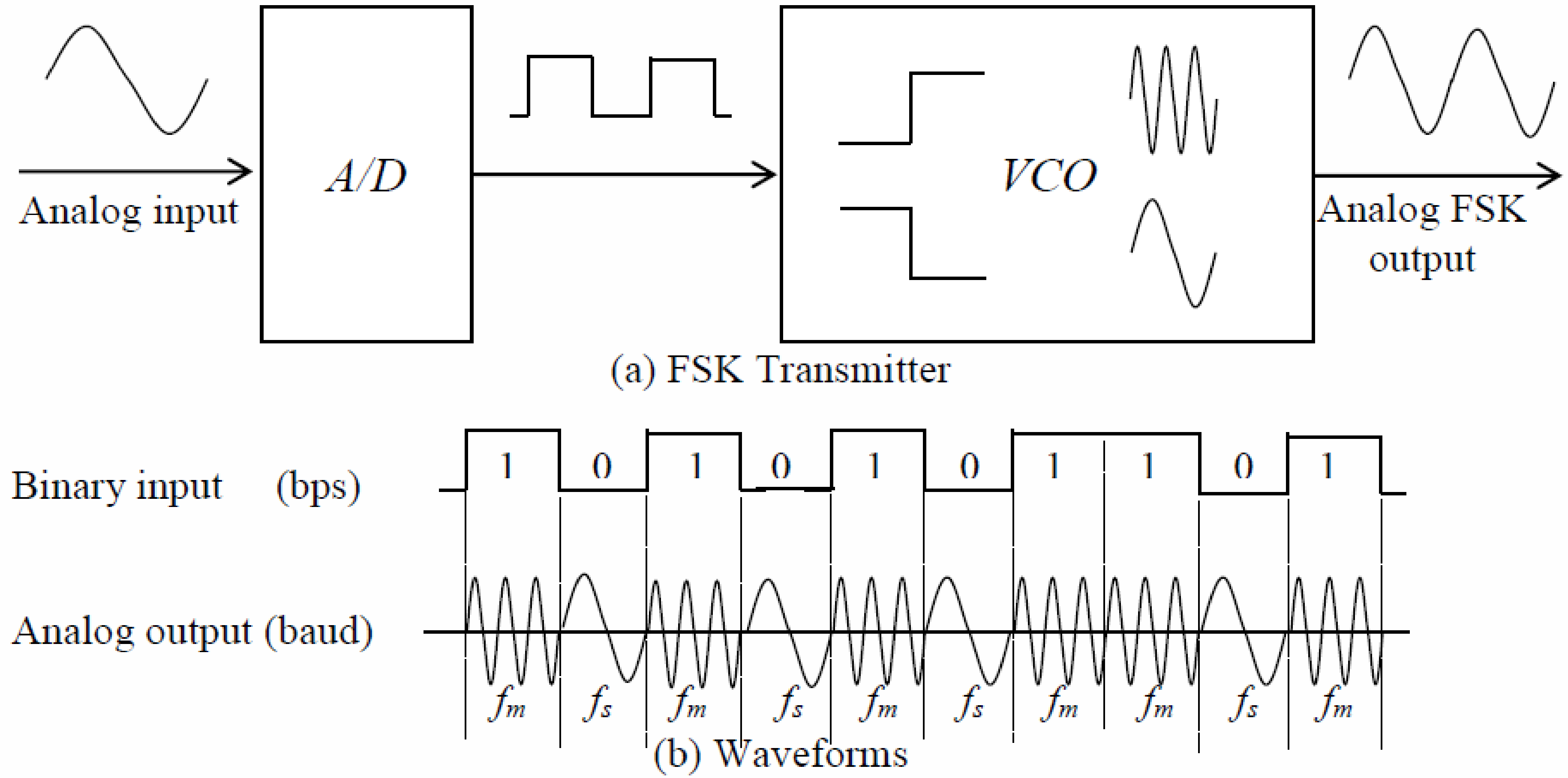
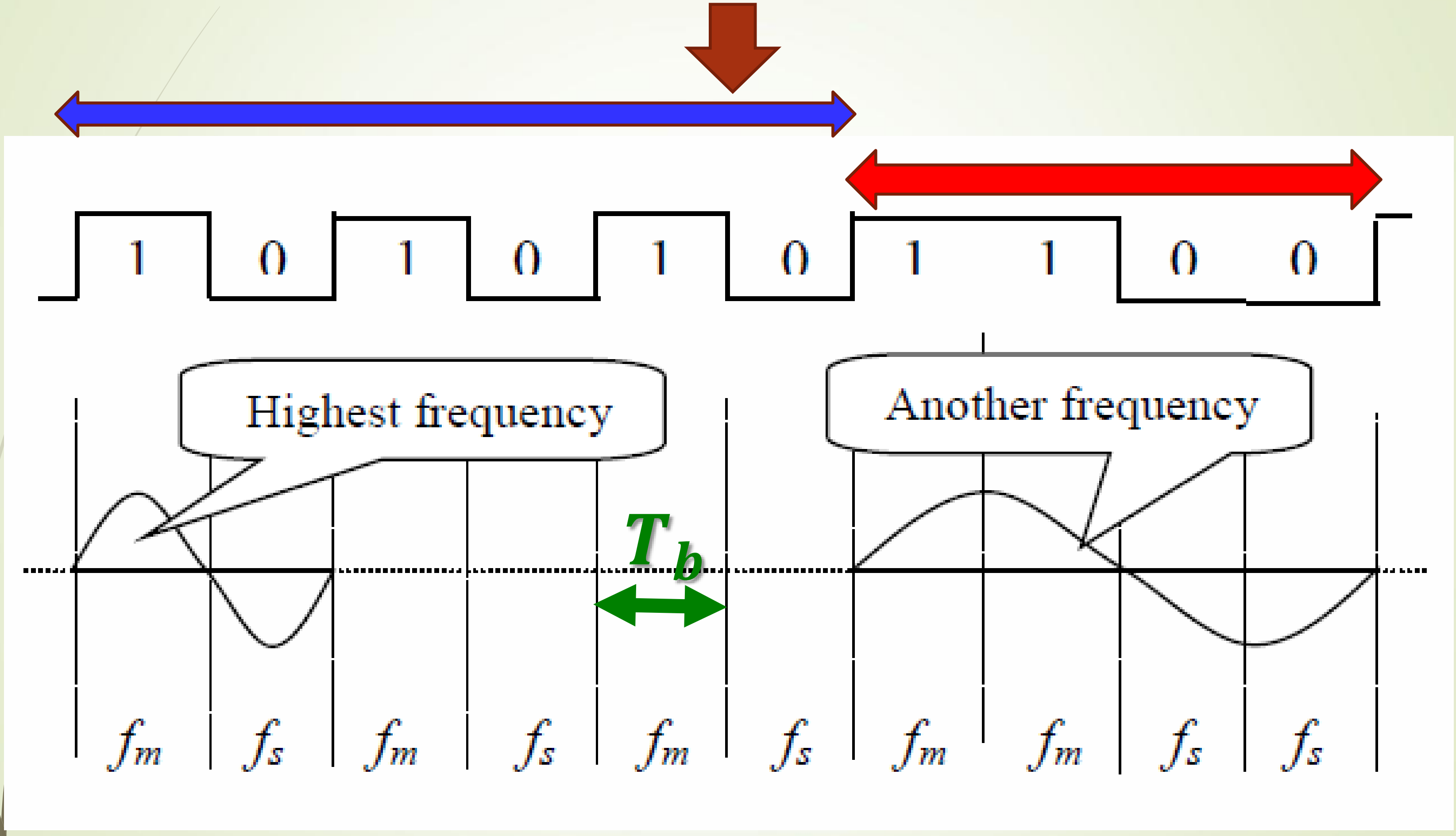


Fig 2.2 Binary FSK Modulator

Bit and Baud Rates

- **Bit rate**, in bits per second,
  - Is the rate of change at the input to the modulator.
- **Baud rate, in symbol per sec**
  - Is the rate of change at the output of the modulator and
  - Is equal to the reciprocal of the time of one output signaling element (termed as symbol).
- So, **baud** is the line speed in symbols per second.

Possible frequencies



Highest Modulating Frequency

- If bit width is T_b, bit rate will be $f_b = \frac{1}{T_b}$
- Fastest rate occurs when input is a series of alternating 1's and 0's:
- If fundamental frequency is considered, highest modulating frequency is one-half the input bit rate.

$$f_m = \frac{f_b}{2}$$

Modulation Index of FSK

- Peak frequency deviation Δf is one half the difference between f_m and f_s:

$$\Delta f = \frac{f_m - f_s}{2}$$

- Formula for modulation index used in FM is also valid for binary FSK as:

$$MI = \frac{\Delta f}{f_m} = \frac{\frac{f_m - f_s}{2}}{\frac{f_b}{2}} = \frac{f_m - f_s}{f_b}$$

- MI is kept below 1.0 for narrow band FM.
- BW is determined from Bessel functions table.
- MI 0.5 and 1.0, either two or three sets of significant side frequencies are generated.
- Thus, minimum BW is two or three times the bit rate.

Bandwidth of Binary FSK

- BW for FSK signal is given by Carson's rule in terms of the frequency deviation and the bandwidth of the digital modulation

$$BW_{FSK} = 2(\Delta f + B)$$

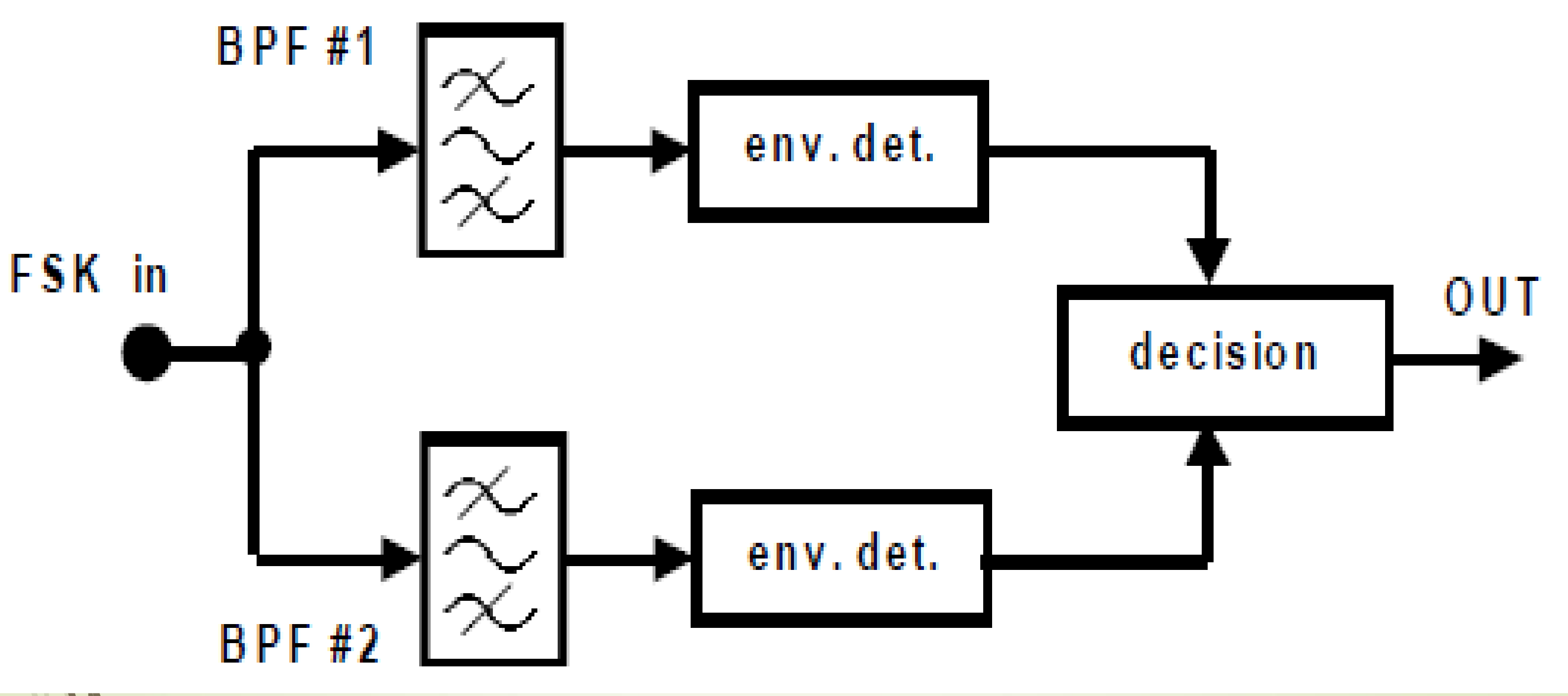
- For alternating 1 and 0, the bandwidth equals the bit rate $B = R$:

$$BW_{FSK} = 2(\Delta f + R)$$

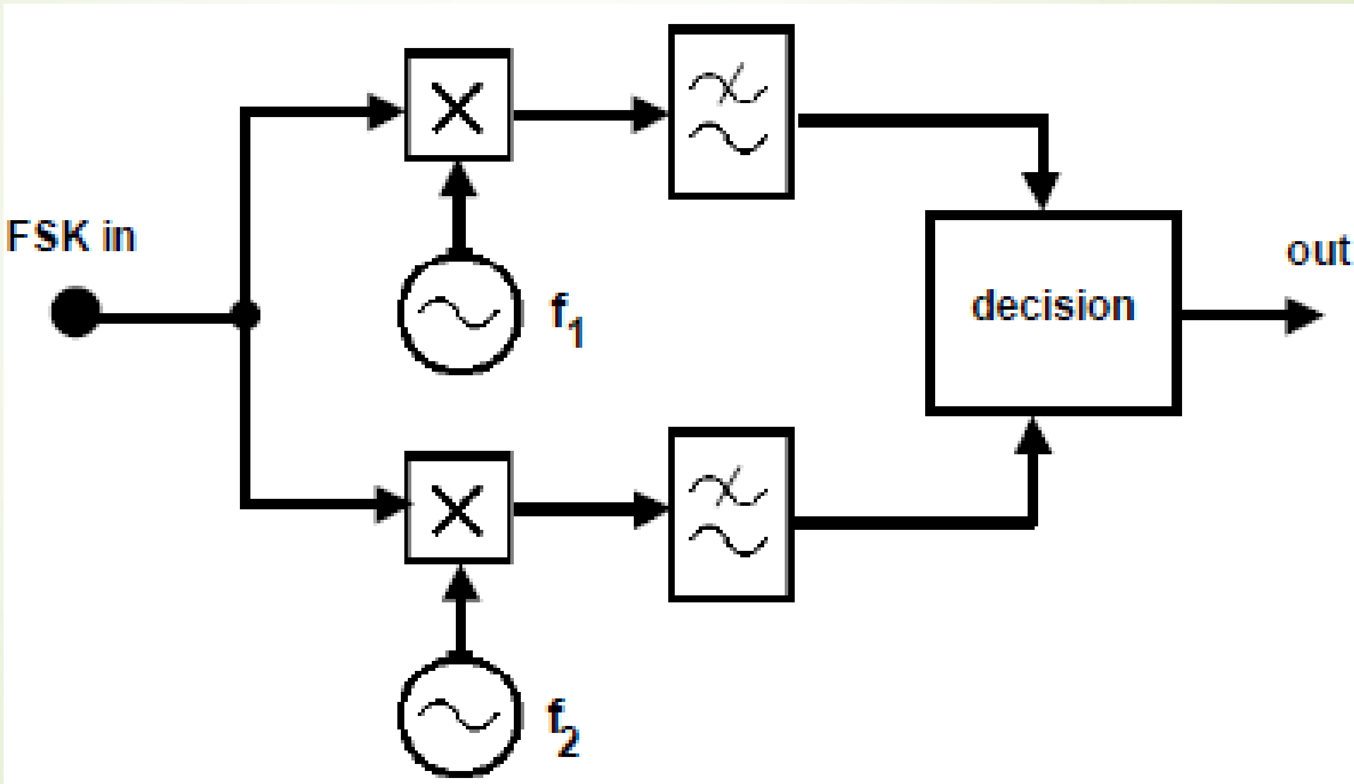
Receiver Binary FSK

- Noncoherent Detection:
  - We do not have knowledge of the carrier.
  - Signal coming is divided into two BPF and envelope detectors.
  - Finally, binary restoration circuit.
- Coherent detection:
  - We need a complete knowledge of the exact carrier frequency on reception.
  - Received signal is applied into two multipliers, at f1 and f0, then to LPF.
  - Finally binary restoration circuit.

FSK
Noncoherent Detector



FSK
Synchronous Detector



Applications of FSK

- Binary FSK has a poorer error performance than PSK or QAM.
- Its use is restricted to low-performance, low-cost, asynchronous data **modems** that are used for **data communication** over analogue, voice band **telephone lines.**

Bell 103-type FSK Modem

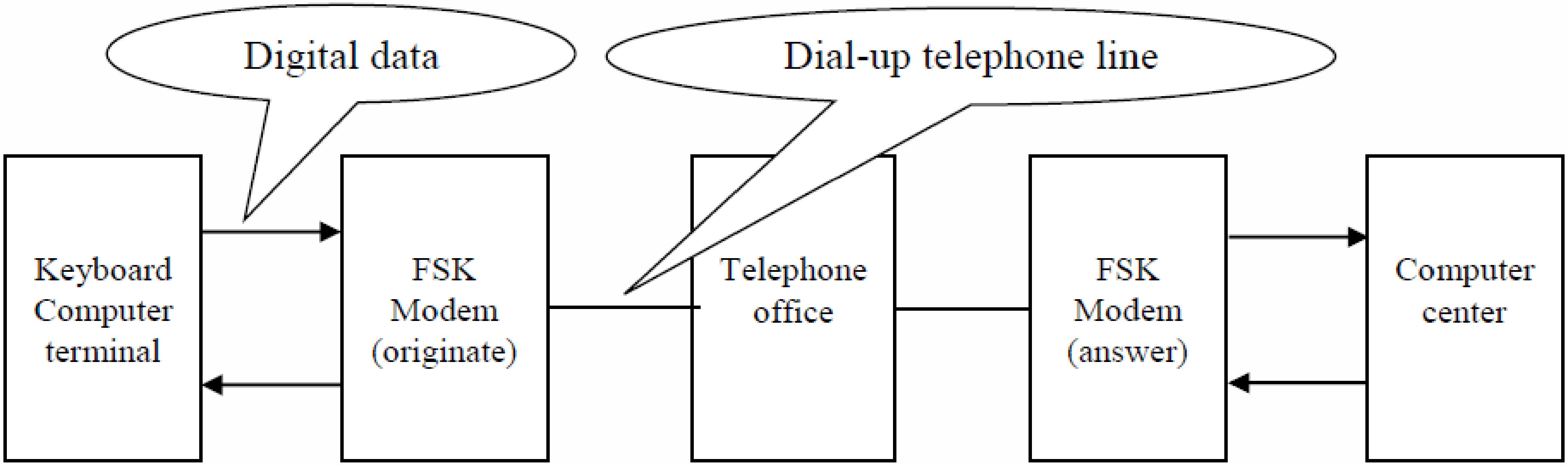


Table 2.1 Mark and Space Frequencies for the Bell Type 103 Modem

	Data	Originate Modem	Answer Modem
Transmit frequencies	Mark (binary 1)	f_1 = 1270 Hz	f_1 = 2225 Hz
	Space (binary 0)	f_2 = 1070 Hz	f_2 = 2025 Hz
Receive frequencies	Mark (binary 1)	f_1 = 2225 Hz	f_1 = 1270 Hz
	Space (binary 0)	f_2 = 2025 Hz	f_2 = 1070 Hz

Bell 103-type FSK Modem

- Keyboard-type computer terminals are often used for communication with a remote computer via dial-up telephone lines.
- Dial-up means that the computer terminal user calls the computer facility on a telephone and uses the telephone connection for data communication.
- Modem (modulator and demodulator) is connected to the phone line at each end as shown
- Two FSK frequency bands are used (one around 1 kHz and another around 2 kHz) so that it is possible to talk and listen simultaneously (full-duplex).
- The standard mark and space frequencies are shown in Table where the peak to peak deviation is $2\Delta F = 200$ Hz

MSK

Minimum Shift Keying

Minimum Shift Keying

- MSK is a continuous phase FSK keying (CPFSK).
- MSK is FSK except mark and space frequencies are synchronized with input binary rate.
- Synchronous means precise time relationship.
- Mark and space frequencies are separated from center frequency by odd multiple of one-half f_b

$$f_m \text{ and } f_s = n\frac{f_b}{2}$$

- MSK has a better bit error performance than FSK for a given signal to noise ratio.
- MSK has less bandwidth than FSK
- However, it requires synchronizing circuits and is therefore more expensive to implement.

MSK versus FSK

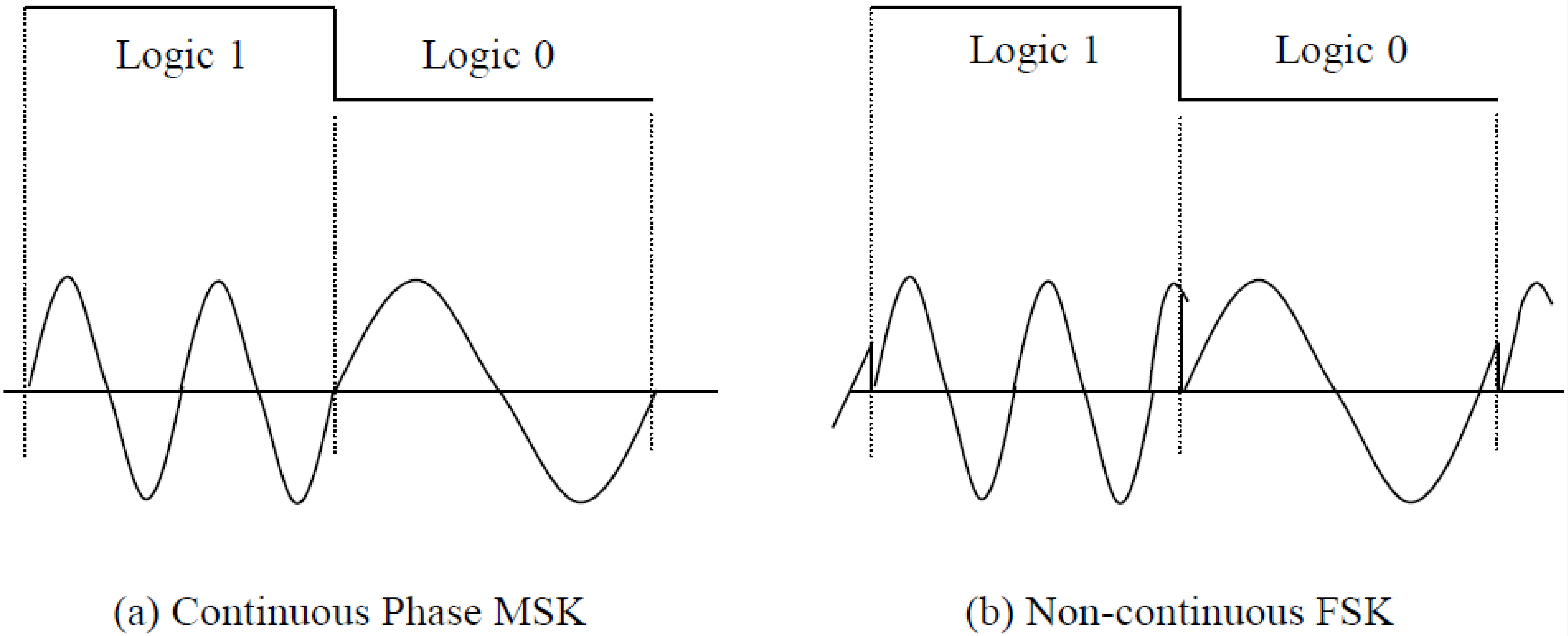


Fig.2.8 Comparison of the Phase Continuity between MSK and FSK

ASK

Amplitude Shift Keying

Amplitude Shift Keying

- In ASK, amplitude of carrier switches between; zero (Off state) and some amplitude (On state)
- Such systems are termed on-off-keyed systems OOK.
- Spectrum of OOK depend on the particular binary sequence to be transmitted. However, the amplitude modulated OOK is the DSB.SC given by:

$$f_{OOK}(t) = f_{ASK}(t) = A\,f(t)\cos\omega_c t$$

- Spectrum of OOK signal is given as:

$$F_{OOK}(\omega) = F_{ASK}(\omega) = \frac{A}{2}\left[F(\omega-\omega_c) + F(\omega+\omega_c)\right]$$

OOK Waveforms

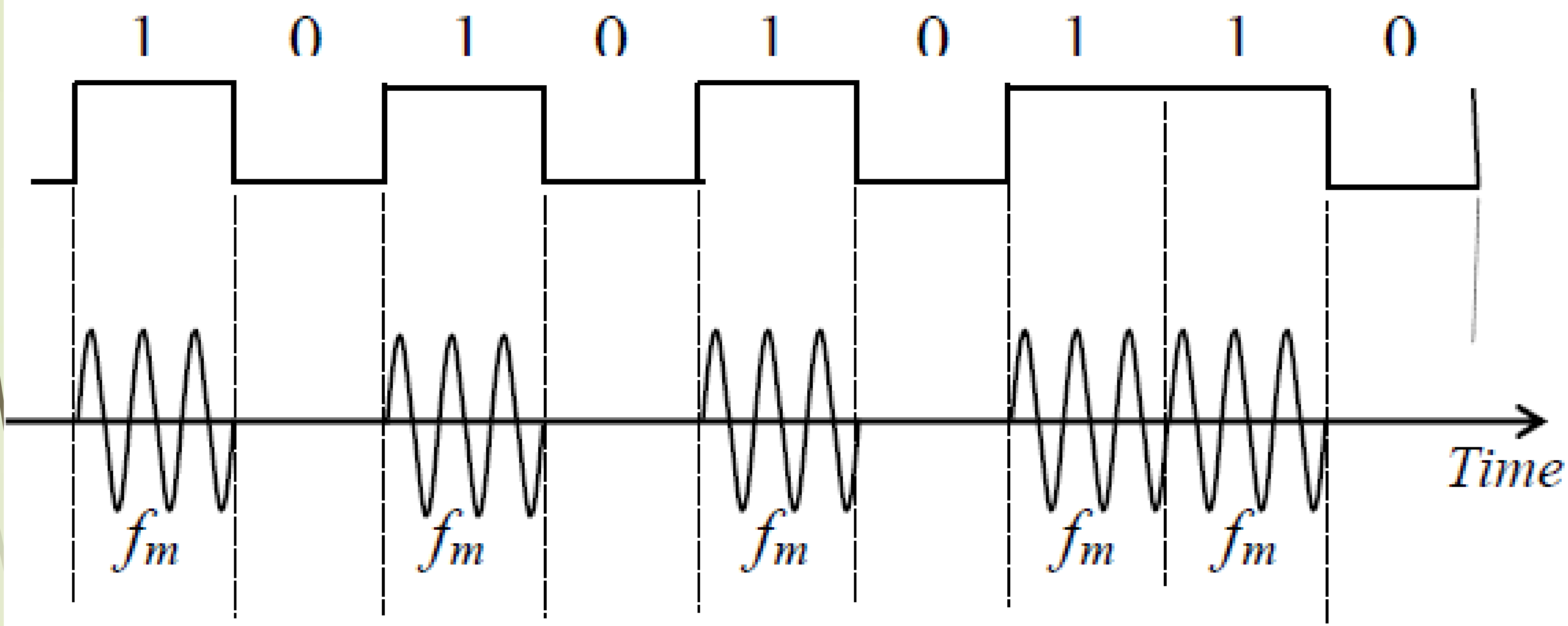


Fig.2.9 ASK or OOK Signal

Spectrum of OOK

- Assume the digital signal *f(t)* is rectangular pulse (special case of binary in which all symbols are 0 except for one 1).

- For a pulse of amplitude *A* and duration *T*, the spectrum of OOK modulator is given by:

$$F_{OOK}(\omega)=\frac{AT}{2}\left[\frac{\sin(\omega-\omega_c)T/2}{(\omega-\omega_c)T/2}+\frac{\sin(\omega+\omega_c)T/2}{(\omega+\omega_c)T/2}\right]=\frac{AT}{2}\left[Sa\left\{\frac{(\omega-\omega_c)T}{2}\right\}+Sa\left\{\frac{(\omega+\omega_c)T}{2}\right\}\right]$$

- For alternating 1's and 0's, spectrum is (sin x) /x.

- So, spectrum of pulse of width *T* and period 2*T* which is translated to frequency f_c as in Fig.2.10

Spectrum of Periodic OOK

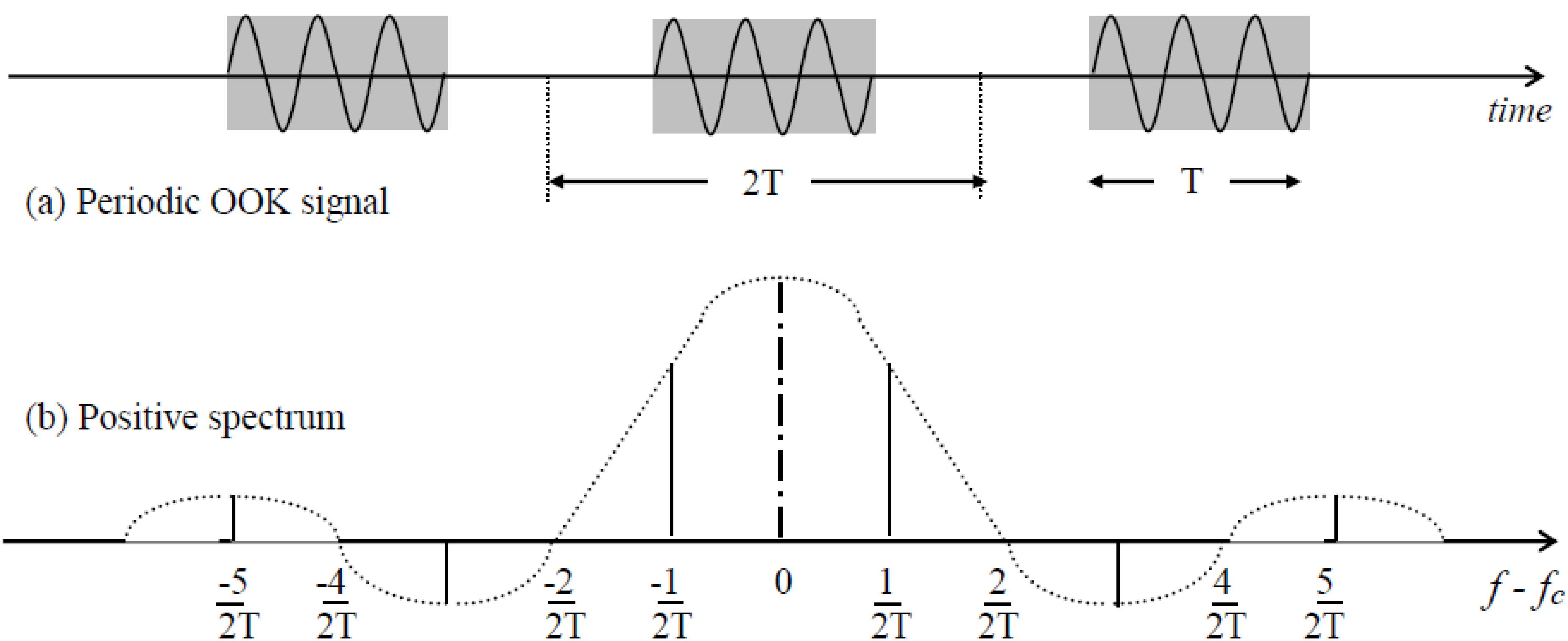


Fig.2.10 Spectrum of Periodic OOK Signal

PSK

Phase Shift Keying

Phase Shift Keying

- PSK is similar to phase modulation PM except that its input gives rise to a limited number of output phases.
- With binary BPSK two output phases are possible for a single carrier frequency. One phase represents a logic 1 and the other represents a logic 0.
- With carrier amplitude V_c and frequency ω_c PSK voltage for binary digital modulating signal *f(t)* is:

$$v(t) = V_c\, f(t) \sin \omega_c t = \begin{cases} +V_c \sin \omega_c t & if \quad f(t) = +1 \\ -V_c \sin \omega_c t & if \quad f(t) = -1 \end{cases}$$

- So, the carrier amplitude remains constant, whereas its phase shifts by 180^o.
- Recall, carrier phase shift rate equals input bit rate.

BPSK Waveforms

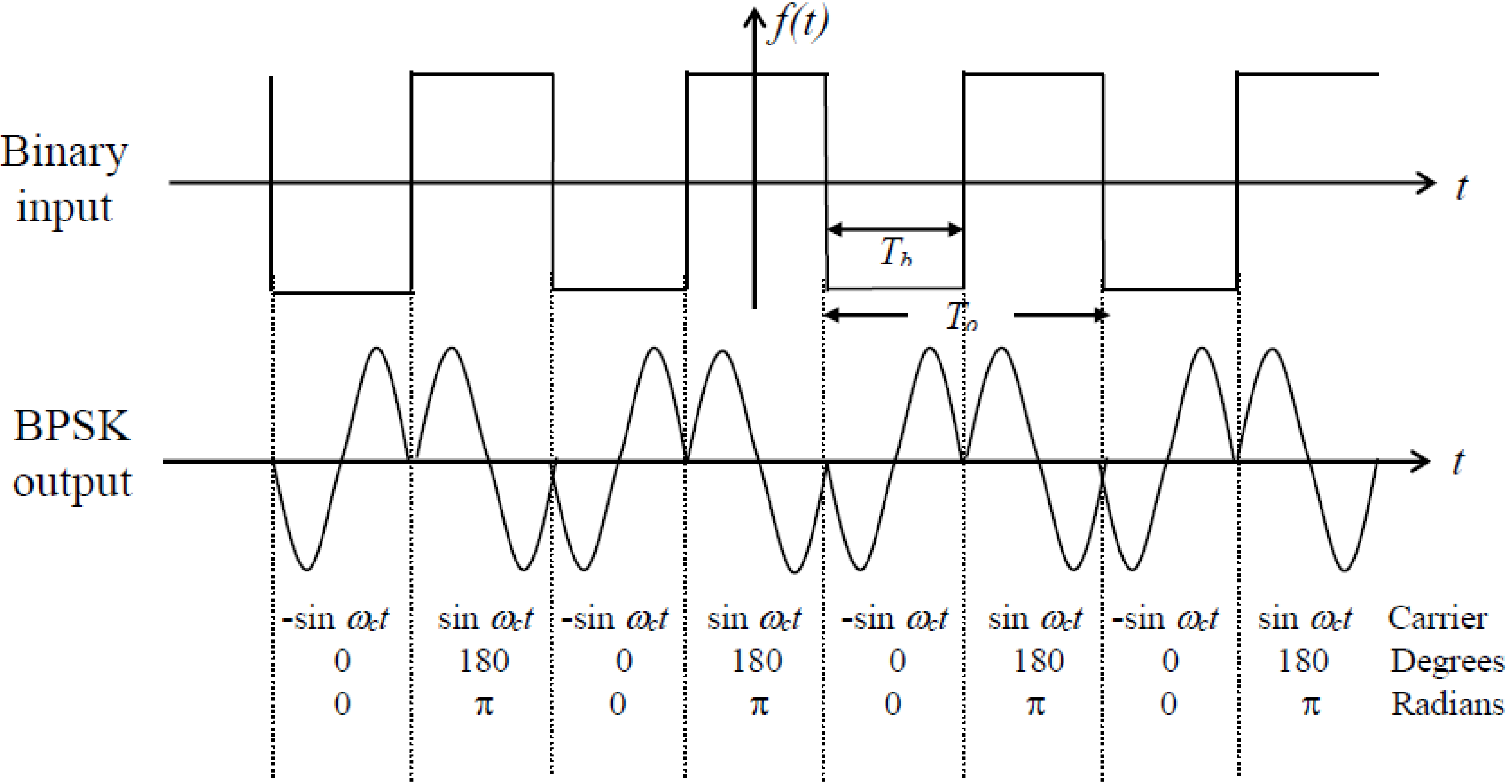


Fig.2.14 Output of BPSK Modulator

PSK Modulator

- Simplified block diagram of BPSK is shown in Fig.2.11
- Balanced modulator acts as a phase reversing switch.
- Carrier is transferred to output either in phase or 180^{o} with respect to reference carrier oscillator.
- Balanced ring modulator circuit is shown in Fig.2.12.
- Digital voltage must be much greater than the peak carrier voltage for proper operation.
  - For logic 1: D1 and D2 are ON while D3 and D4 are OFF, carrier voltage across T2 is in phase with the carrier voltage across T1 or the reference oscillator.
  - For logic 0: D1 and D2 are OFF while D3 and D4 are ON, carrier voltage across T2 is 180^{o} out of phase with reference oscillator.

Transmitter of BPSK

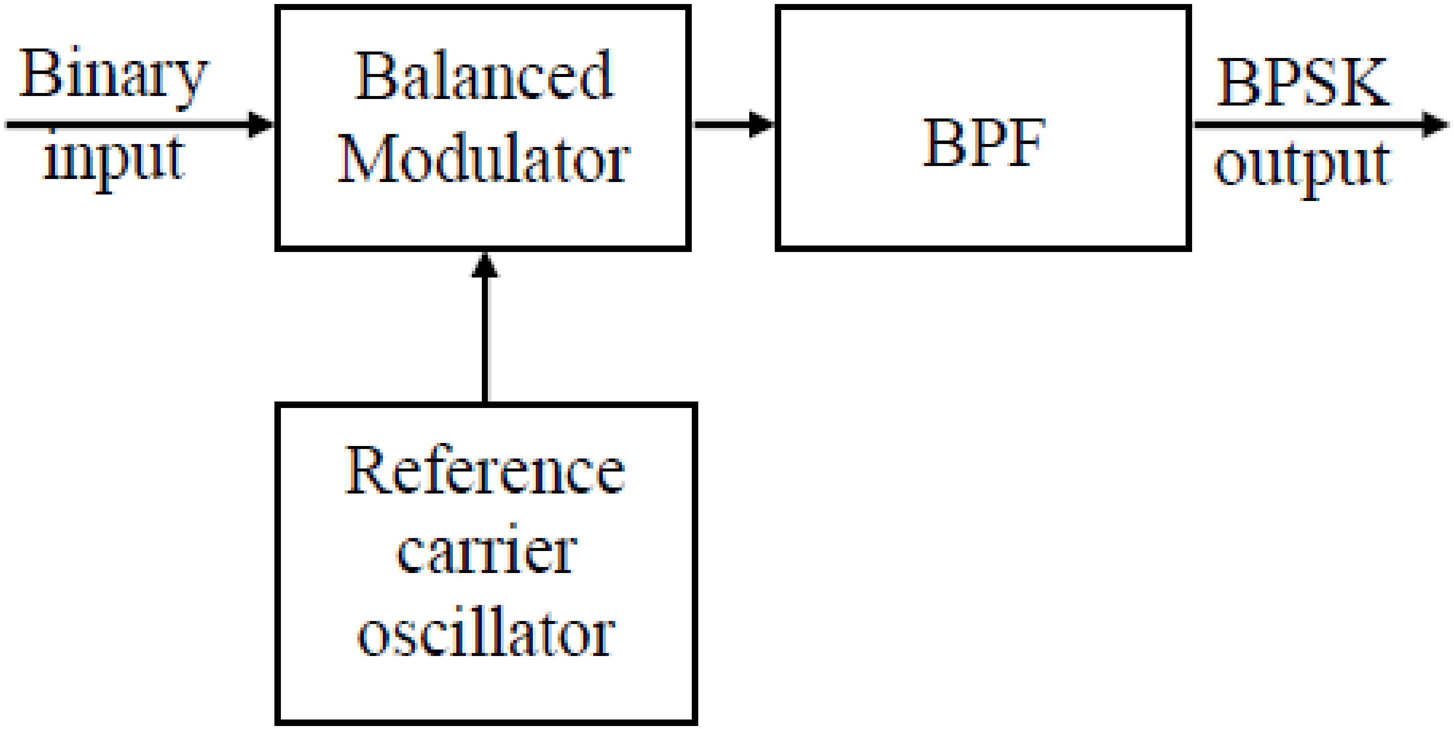


Fig.2.11 BPSK Modulator

PSK Balanced Ring Modulator

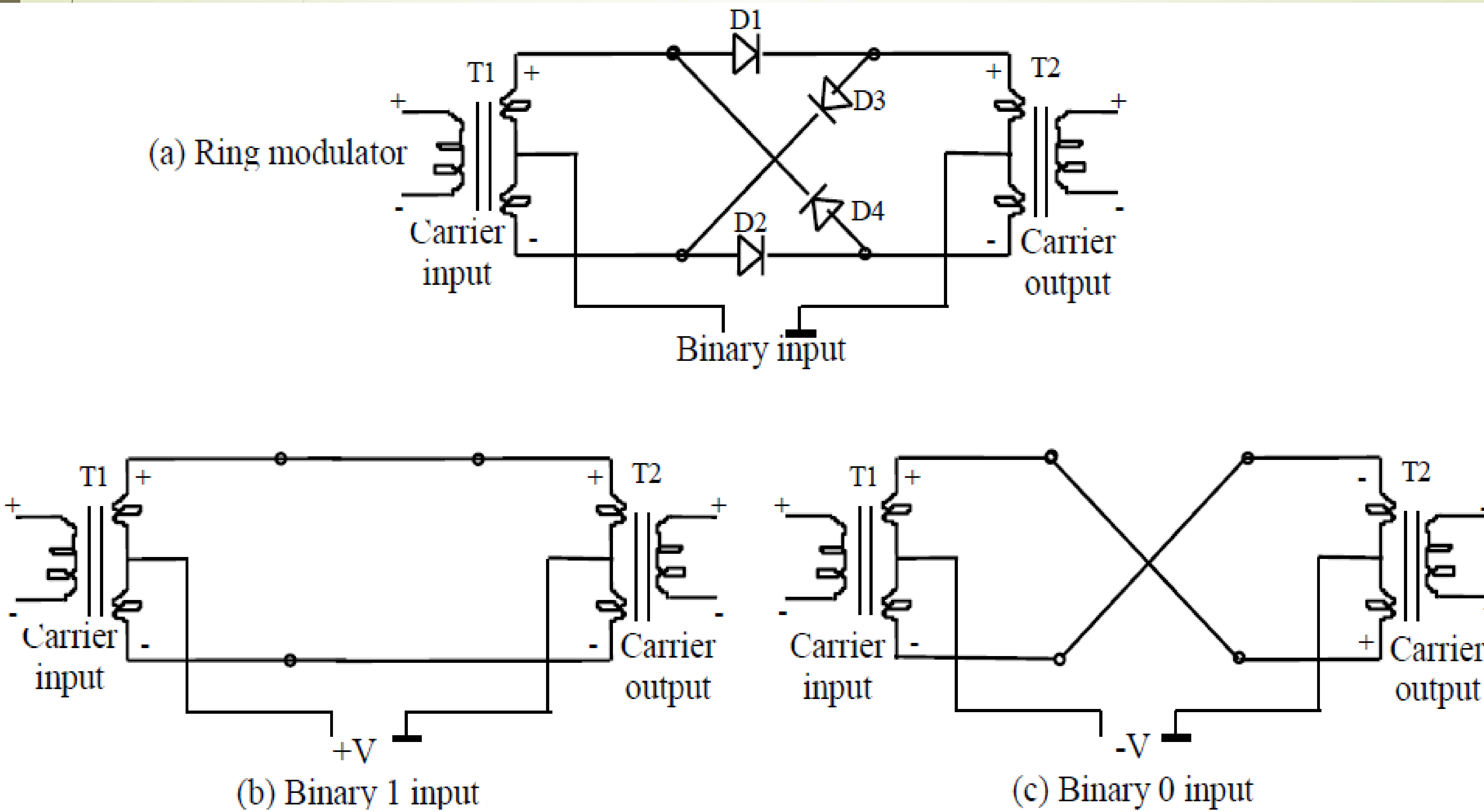


Fig.2.12 Balanced Ring Modulator

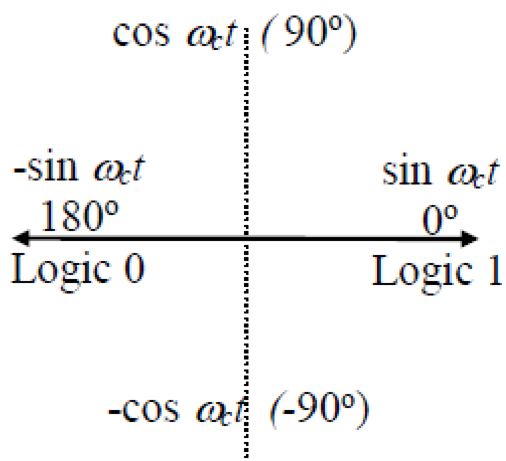
Representation of BPSK

- Figure shows truth table, phasor diagram and constellation diagram for a BPSK.
- Constellation diagram is similar to phasor except that the entire phasor is not drawn.
- Only the relative positions of the peaks of the phasors are shown.

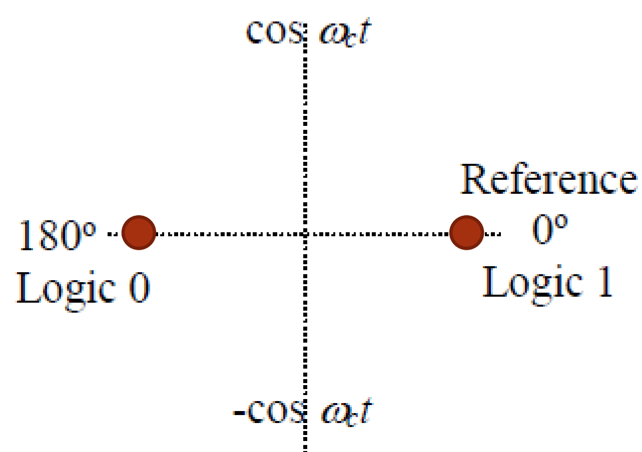
Truth, Phasor, Constellation

Binary input	Output phase
Logic 0	180°
Logic 1	0°

(a) Truth table



(b) Phasor diagram



(c) Constellation diagram

Fig.2.13 BPSK Representation

Band Width of PSK

- Balanced modulator is product so carrier is multiplied by binary data (either +1 or –1).
- Also, widest bandwidth occurs when data is alternating 1/0 sequence.
- Product modulator output of the BPSK is:

$$output = \sin \omega_a t \sin \omega_c t = \frac{1}{2}\cos(\omega_c - \omega_a)t + \frac{1}{2}\cos(\omega_c + \omega_a)t$$

- Consequently, minimum double-sided Nyquist bandwidth is:

$$B_{BPSK} = (\omega_c + \omega_a) - (\omega_c - \omega_a) = 2\omega_a = 2(f_b/2) = f_b$$

- Minimum bandwidth to pass worst-case BPSK equals input bit rate.

PSK Reception

- Simple block diagram of BPSK detection.

- Coherent carrier recovery circuit detects and regenerates carrier that is both frequency and phase coherent with the original transmit carrier.

- Balanced modulator output is the product of two inputs (BPSK signal and the recovered carrier).

- The LPF separates the recovered binary data from the complex demodulated spectrum.

Detection of BPSK

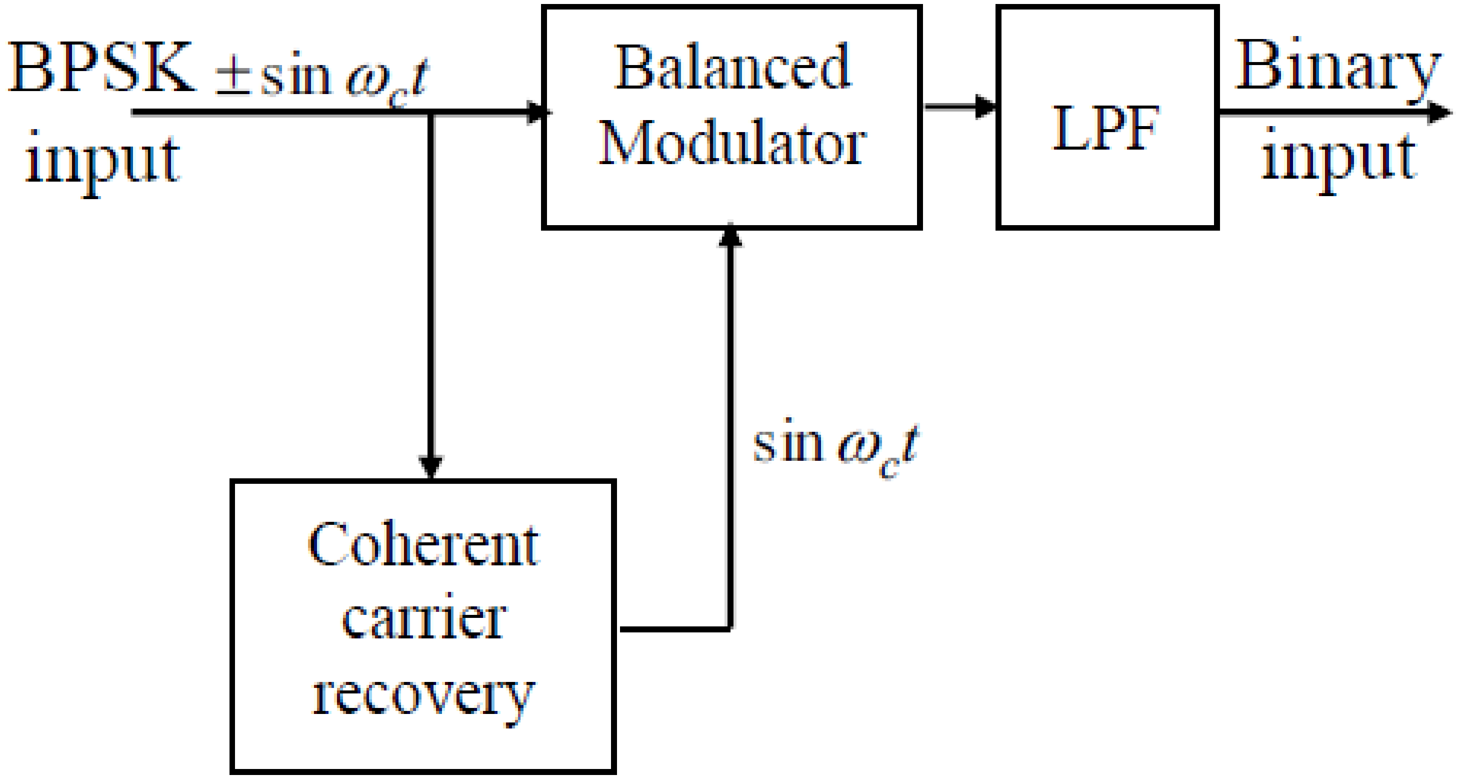


Fig.2.15 BPSK Receiver

Demodulation Process

- For input +*sin* $w_c t$ (logic 1), balanced output is:

$$Output = \sin\omega_c t \sin\omega_c t = \sin^2\omega_c t = \frac{1}{2}\left(1-\cos 2\omega_c t\right) = \frac{1}{2} - \frac{1}{2}\cos 2\omega_c t$$

$$Filter\,output = +\frac{1}{2} \quad dc\,voltage \equiv Logic\,1$$

- For input -*sin* $w_c t$ (logic 0), the output is:

$$Output = -\sin\omega_c t \sin\omega_c t = -\sin^2\omega_c t = -\frac{1}{2}\left(1-\cos 2\omega_c t\right) = -\frac{1}{2} + \frac{1}{2}\cos 2\omega_c t$$

$$Filter\,output = -\frac{1}{2} \quad dc\,voltage \equiv Logic\,0$$

M-ary Phase Shift Keying

M-ary Encoding

- In M-ary, one of M possible signals may be transmitted during each signaling interval.
- It is advantageous to encode at a level higher than binary, e.g., **4**PSK and **8**PSK.
- Each possible transmitted signal of an M-ary message sequence is referred to as "**symbol**".
- Mathematically, the number of bits per symbol n is related to the number of possible signals M by:

$$M = 2^n$$

-

Quadrature PSK

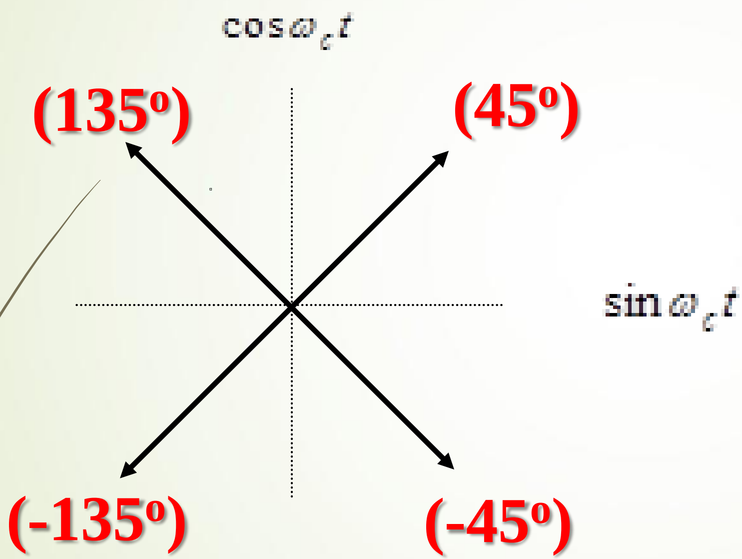
- QPSK, is another form of angle modulated, constant envelope digital modulation, and $M = 4$ possible symbols.
- 4 phases are possible for a single carrier frequency.
- Binary input data are combined into groups of 2 bits called dibits.
- Each dibit code generates one of the four possible output phases.
- For each 2- bit, a single output change occurs. So, the output baud rate is one-half of the input bit rate.
-

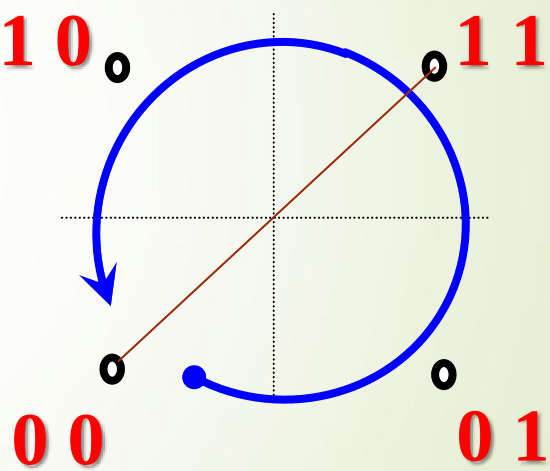
QPSK Truth Table

Inputs		Output
A	B	Phase
0	0	-135
0	1	-45
1	0	+135
1	1	+45

QPSK

Phasor Constellation





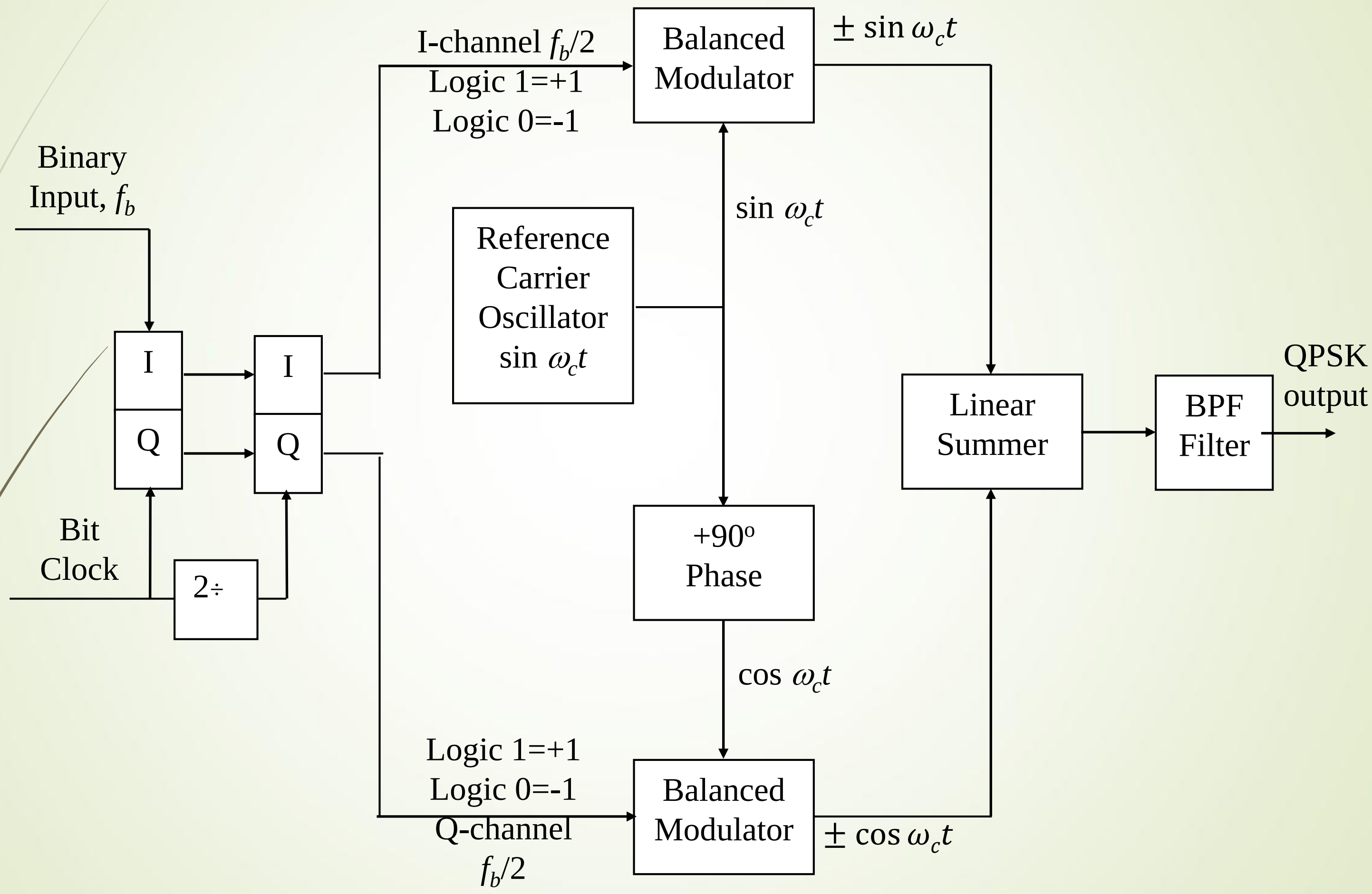
0 0

0 1

1 1

1 0

QPSK Transmitter



Transmitter Operation

- QPSK modulator is a two BPSK modulators combined in parallel.
- Two bits are clocked into the bit splitter.
- After both bits have been serially inputted, they are simultaneously parallel outputted.
- One bit is directed to I-channel to modulate the carrier that is in phase with the reference.
- Other bit is directed to Q-channel to modulate carrier that is 90^{o} out of phase or in quadrature with the reference.
- If linear summer combines the two quadrature signals, there are 4 possible phases as follows:

$$\pm \sin \omega_c t \pm \cos \omega_c t$$

Splitting to I and Q Channels

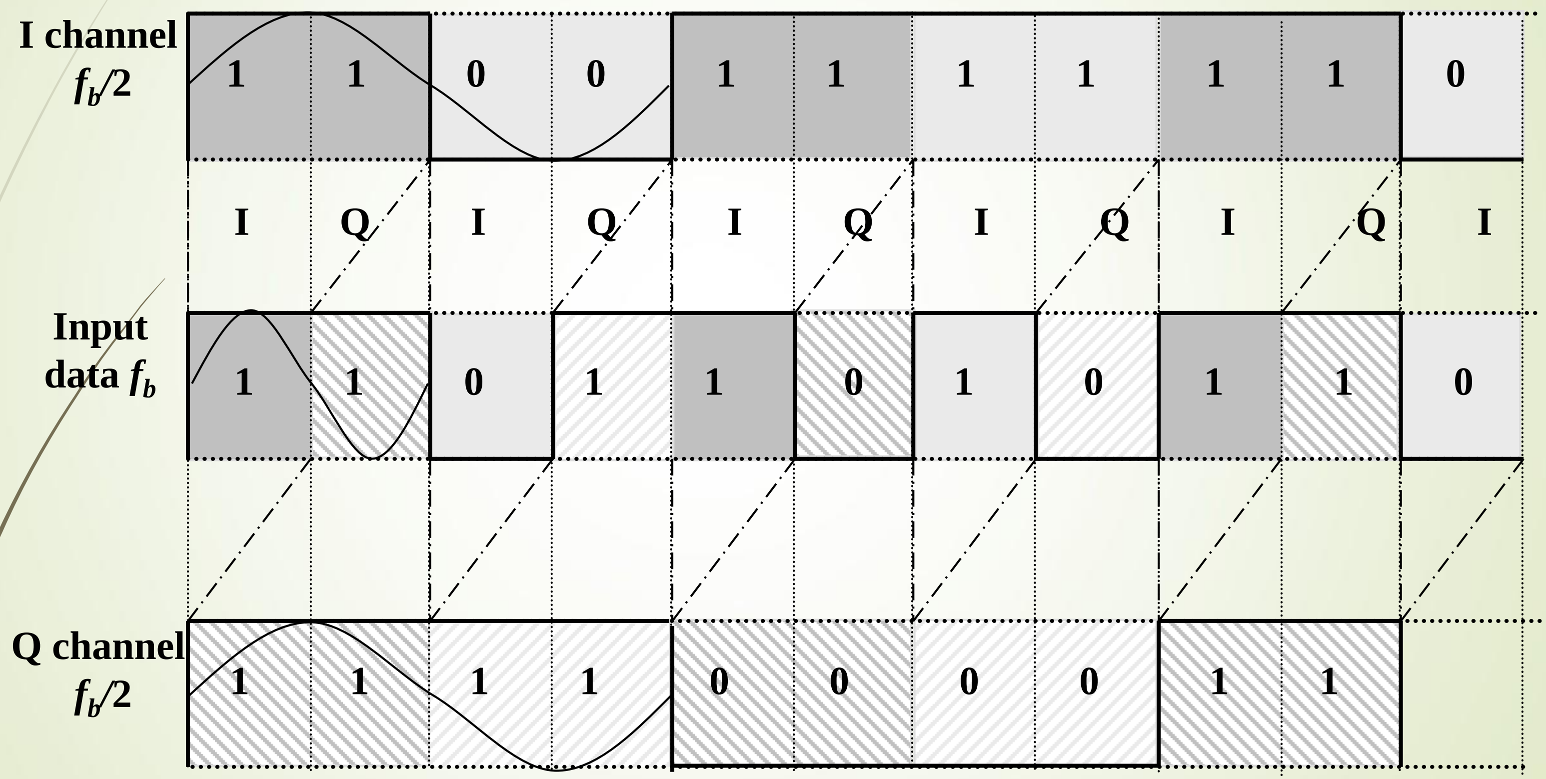


Fig.3.16: Highest Fundamental Frequency

Bandwidth of QPSK

- Input data rate f_b is divided into two channels.
- I or Q channel bit rate is ½ input rate, i.e., $f_b/2$.
- Highest fundamental frequency at input of balanced modulators is one-fourth of input rate, i.e., $f_b/4$
- Balanced modulator product of I or Q channels:

$$\boldsymbol{Output} = \sin \omega_a t \sin \omega_c t = \sin 2\pi \frac{f_b}{4} t \sin 2\pi f_c t$$

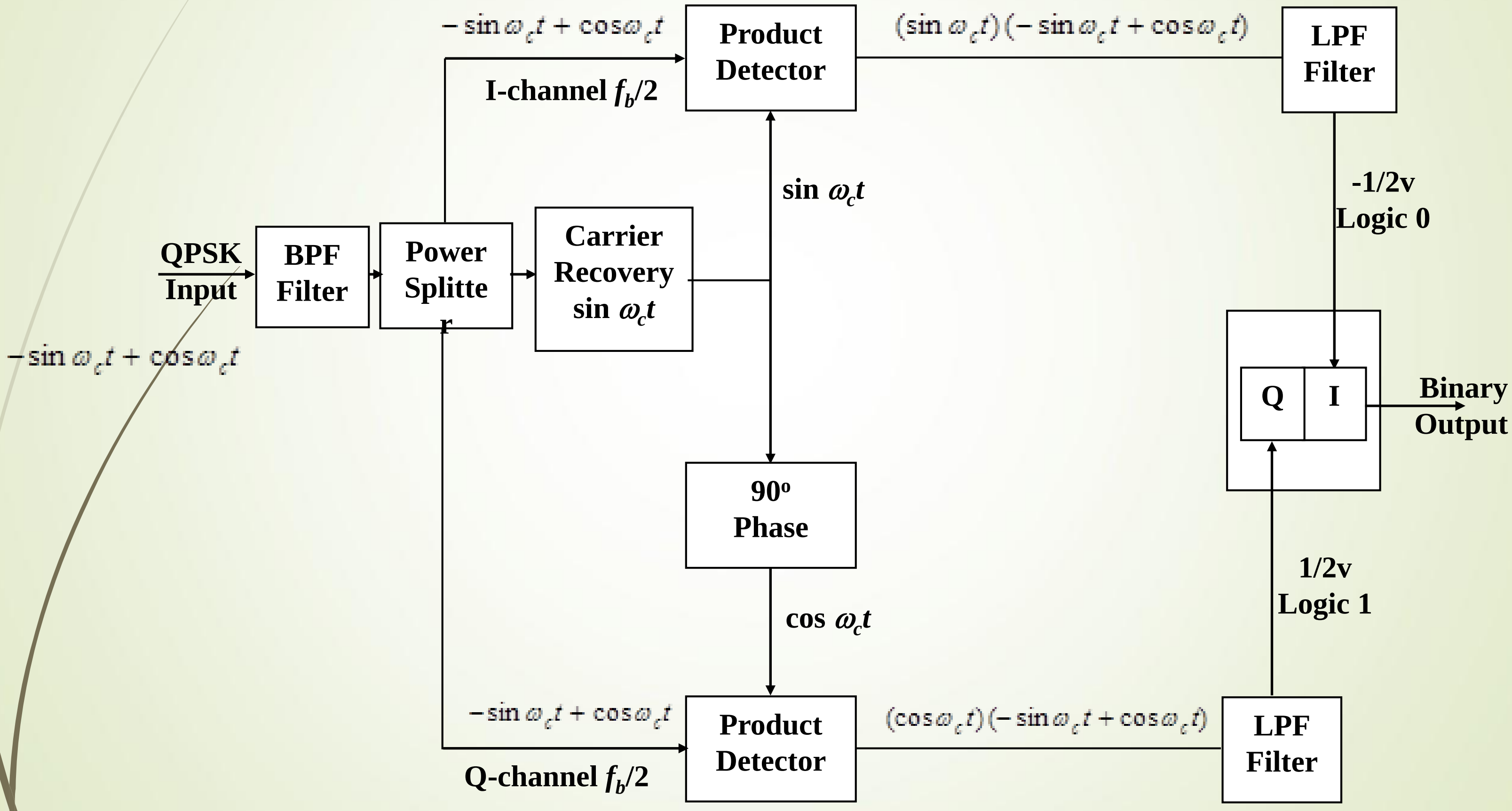
$$\boldsymbol{Output} = \sin 2\pi \left(f_c - \frac{f_b}{4} \right) t \sin 2\pi \left(f_c + \frac{f_b}{4} \right) t$$

- So, output extends from fc-fb/4 up to fc+fb/4:

$$\boldsymbol{BW_{QPSK}} = f_c + \frac{f_b}{4} - \left(f_c - \frac{f_b}{4} \right) = \frac{f_b}{2}$$

- Minimum bandwidth of QPSK is less than incoming rate so that bandwidth is compressed to $f_b/2$ only.

QPSK Receiver



Receiver Operation

- Power splitter directs QPSK signal into I and Q channels and carrier recovery circuit.
- Carrier recovery circuit reproduces the original transmit reference carrier.
- QPSK signal is demodulated in I and Q channels through product detectors.
- Detectors outputs are fed to combining circuit, to convert from parallel I and Q channels to a single binary output.

Offset QPSK [OQPSK]

A modified form of QPSK where the bit waveforms on I and Q channels are offset or shifted in phase by one-half of a bit time.

- It can be implemented by adding a delay.
- In QPSK, change from 00 to 11 or 01 to 10 causes 180° shift in output phase.
- Since changes in I channel of OQPSK occur at midpoints of Q bits, there is never more than a single bit change in the dibit code,
- So, 90° shift in phase improves performance.
- Disadvantage: changes in phase occur at twice the data rate so bandwidth is twice.

OQPSK Transmitter

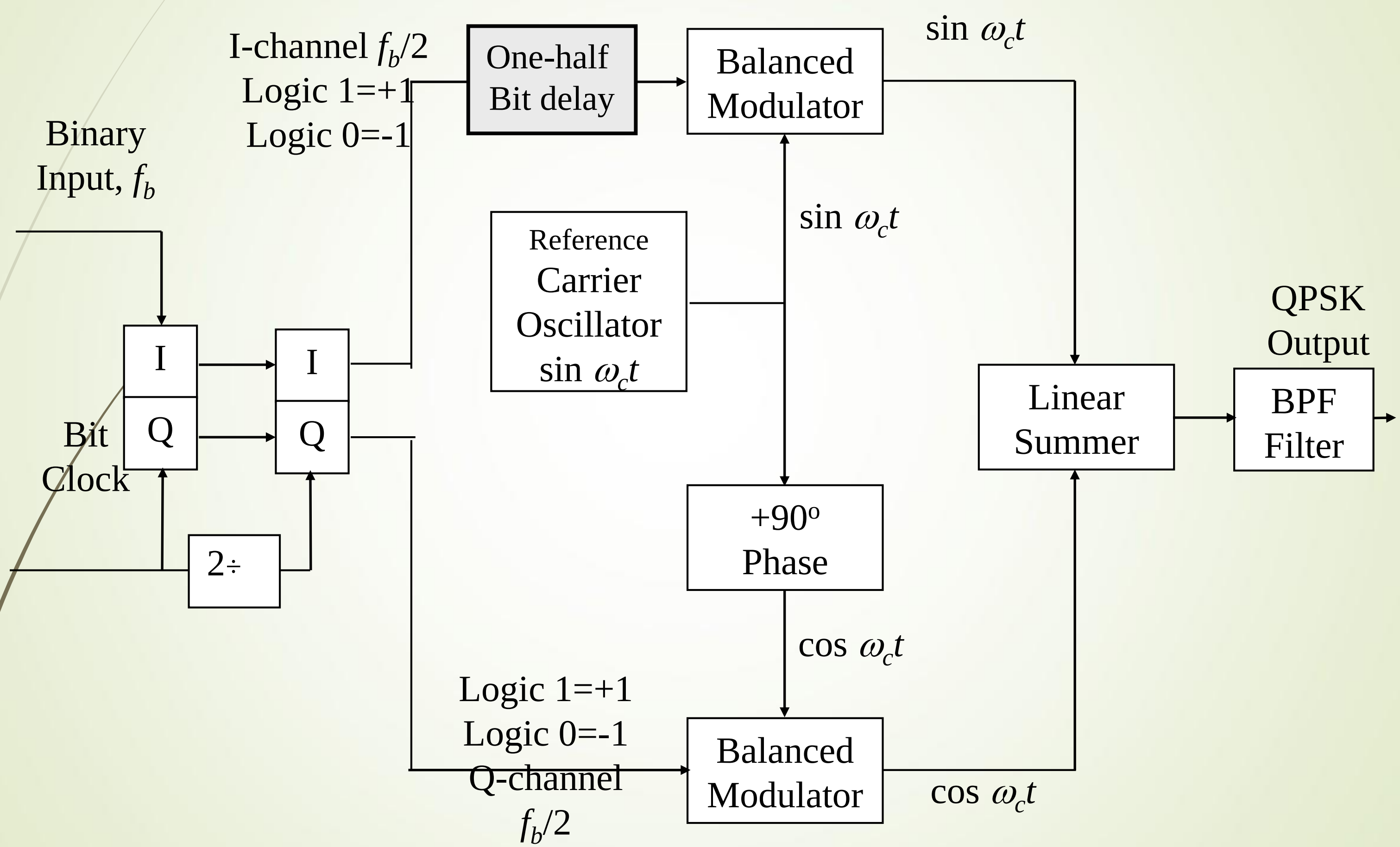
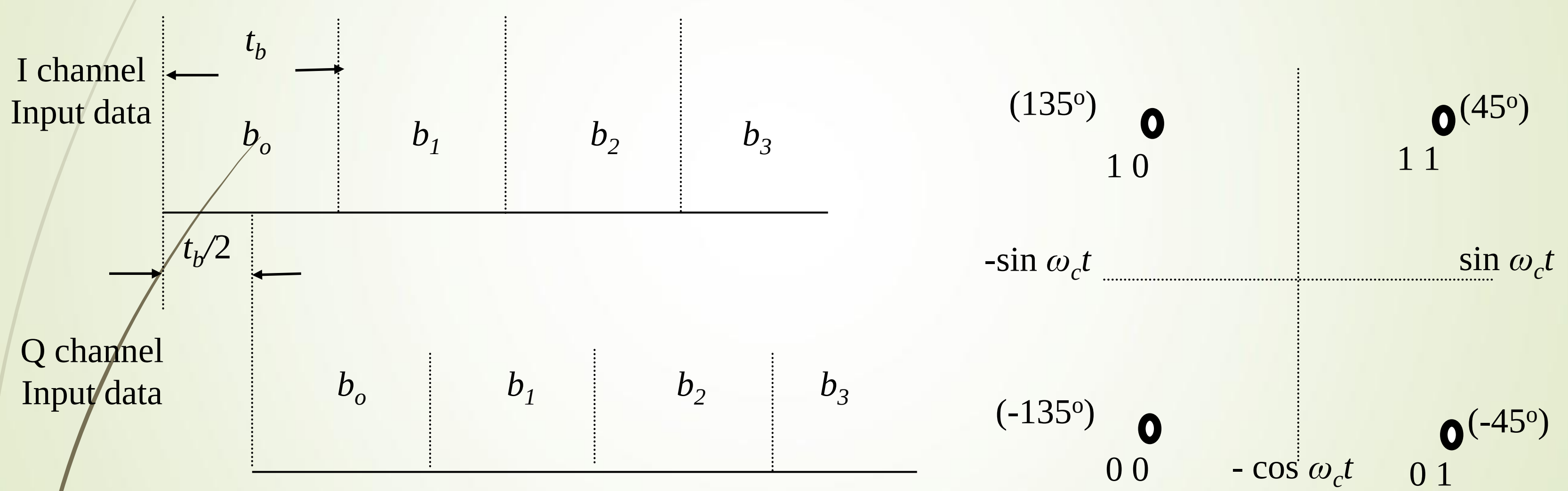


Fig.3.18: Offset QPSK Modulator

Offset Delay Concepts



(a) Bit sequence alignment (b) Constellation diagram

Fig.3.19: OQPSK

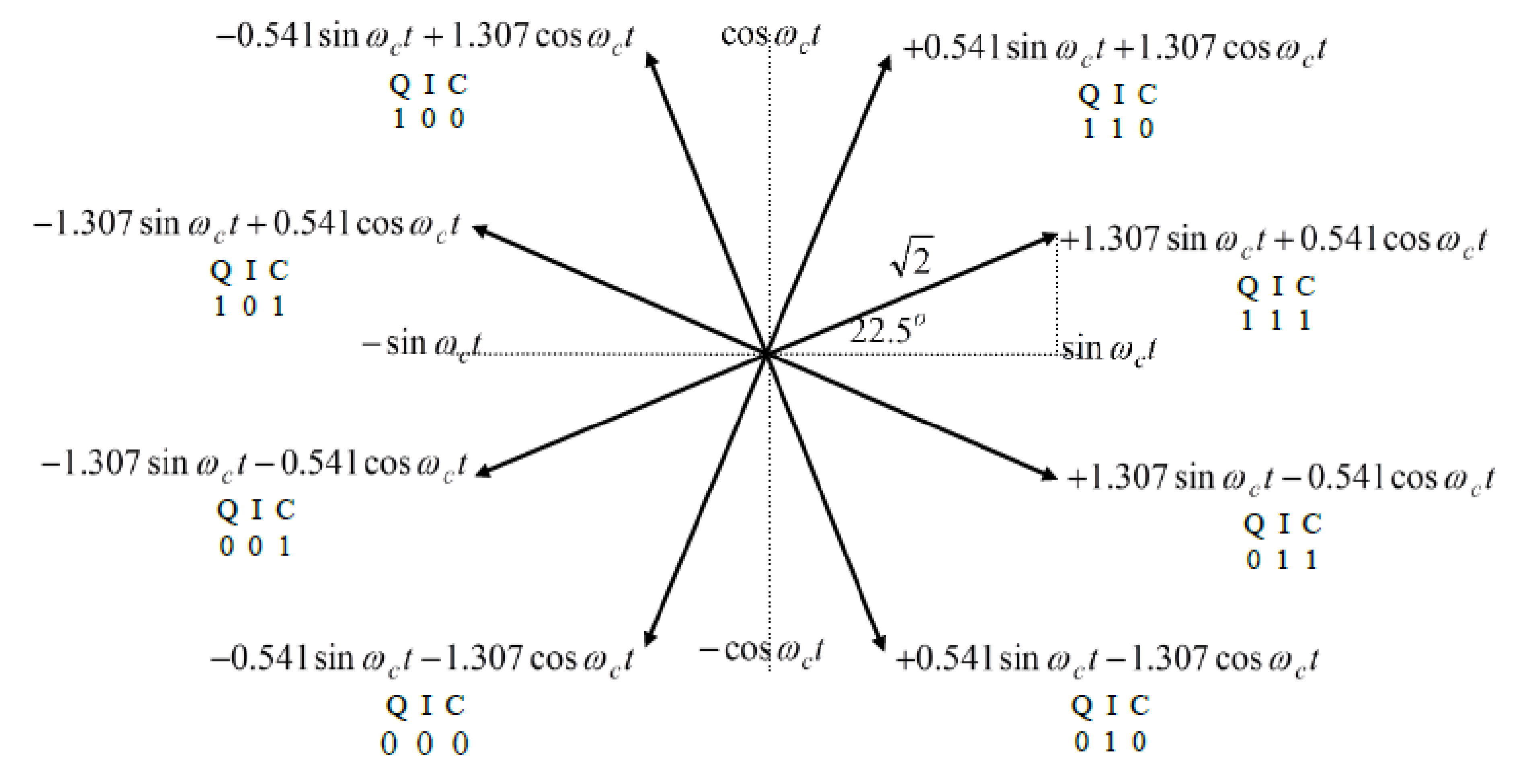
8 PSK

Eight Phase PSK

Phases of 8 PSK:

- $\Delta\emptyset = \frac{2\pi}{8} = \frac{\pi}{4} = \mathbf{45^o}$
- $\textbf{First phasor} = \frac{\Delta\emptyset}{2} = \frac{45}{2} = \mathbf{22.5^o}$
- $\textbf{Second} = \textbf{First} + \Delta\emptyset = 22.5 + 45 = \mathbf{67.5^0}$
- $\boldsymbol{Third} = \boldsymbol{Second} + \Delta\emptyset = 67.5 + 45 = \mathbf{112.5^0}$
- $\textbf{Last} = \textbf{First} + (n-1)\Delta\emptyset = 22.5 + 7 * 45 = \mathbf{337.5}$

8PSK Phasor

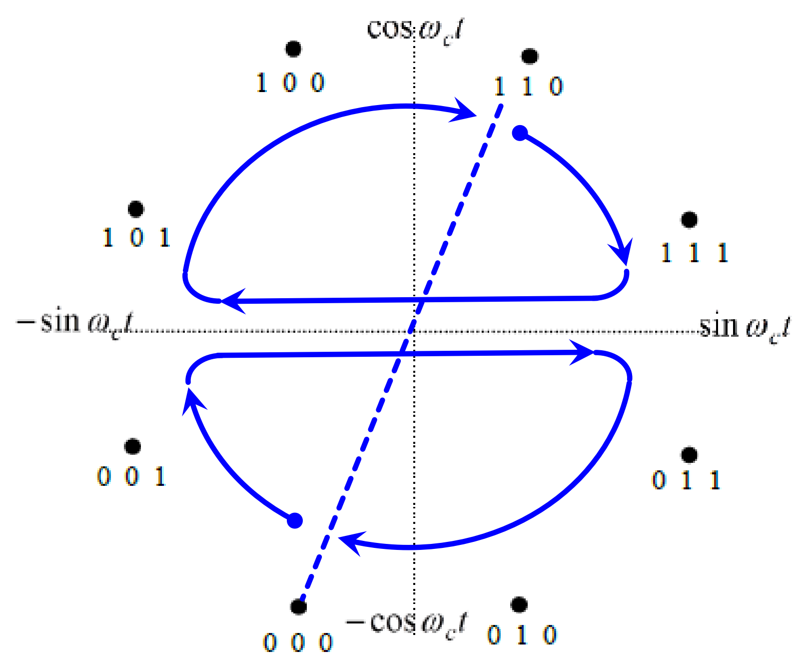


$-0.541\sin\omega_c t + 1.307\cos\omega_c t$
Q I C
1 0 0
$\cos\omega_c t$
$+0.541\sin\omega_c t + 1.307\cos\omega_c t$
Q I C
1 1 0
$-1.307\sin\omega_c t + 0.541\cos\omega_c t$
Q I C
1 0 1
$\sqrt{2}$
$+1.307\sin\omega_c t + 0.541\cos\omega_c t$
Q I C
1 1 1
22.5^o
$-\sin\omega_c t$
$\sin\omega_c t$
$-1.307\sin\omega_c t - 0.541\cos\omega_c t$
Q I C
0 0 1
$+1.307\sin\omega_c t - 0.541\cos\omega_c t$
Q I C
0 1 1
$-0.541\sin\omega_c t - 1.307\cos\omega_c t$
Q I C
0 0 0
$-\cos\omega_c t$
$+0.541\sin\omega_c t - 1.307\cos\omega_c t$
Q I C
0 1 0

8PSK Truth - Constellation

Binary input			8-PSK Output phase
Q	I	C	
0	0	0	-112.5
0	0	1	-157.5
0	1	0	-067.5
0	1	1	-022.5
1	0	0	+112.5
1	0	1	+157.5
1	1	0	+067.5
1	1	1	+022.5

(b) The Truth Table of 8-PSK



(c) Constellation diagram of 8-PSK

0 0 0
0 0 1
0 1 1
0 1 0
1 1 0
1 1 1
1 0 1
1 0 0

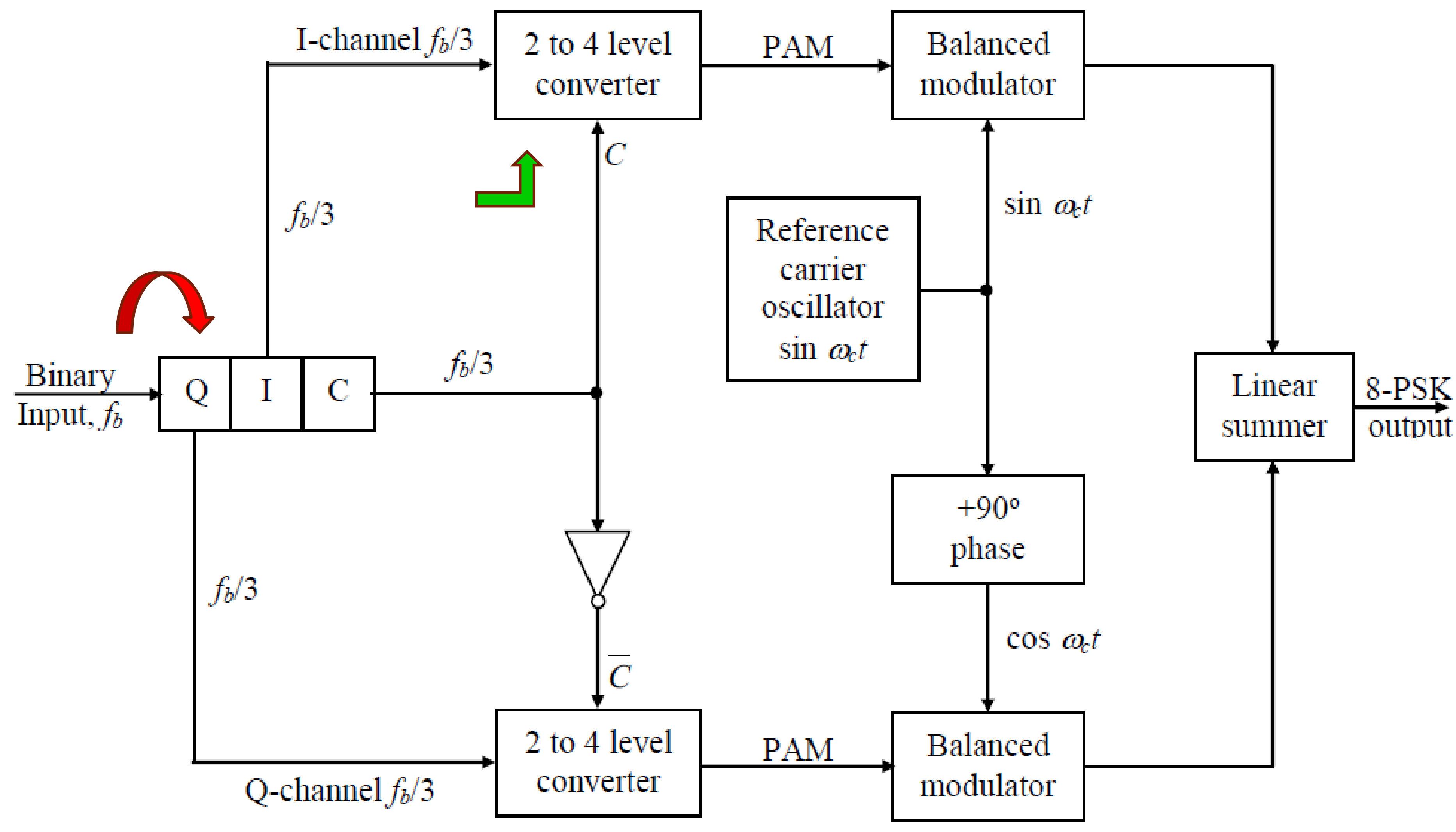
8 PSK Transmitter

- **Serial to Parallel (Bit Splitter):**

  Converts binary input into 3 parallel channels:

  - **In Phase** Channel, ‘I’
  - **Quadrature** Channel ‘Q’
  - **Control** Channel ‘C’

8PSK Transmitter



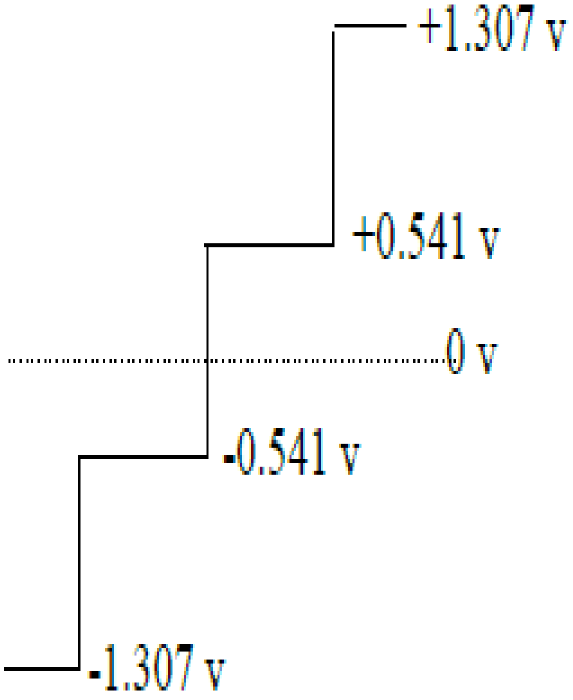
2-4 Converter

- Digital to Analogue Converter
  - I and C bits are inputs of DAC of I-Channel
  - Q and $\overline{C}$ are inputs of DAC of Q-Channel
- With 2 parallel input bits, 4 output voltages are possible
  - I or Q bits gives polarity of analogue output
  - C or $\overline{C}$ bits gives magnitude of output:
    - Logic 1: Magnitude is 1.307 v
    - Logic 0: Magnitude is 0.541 v

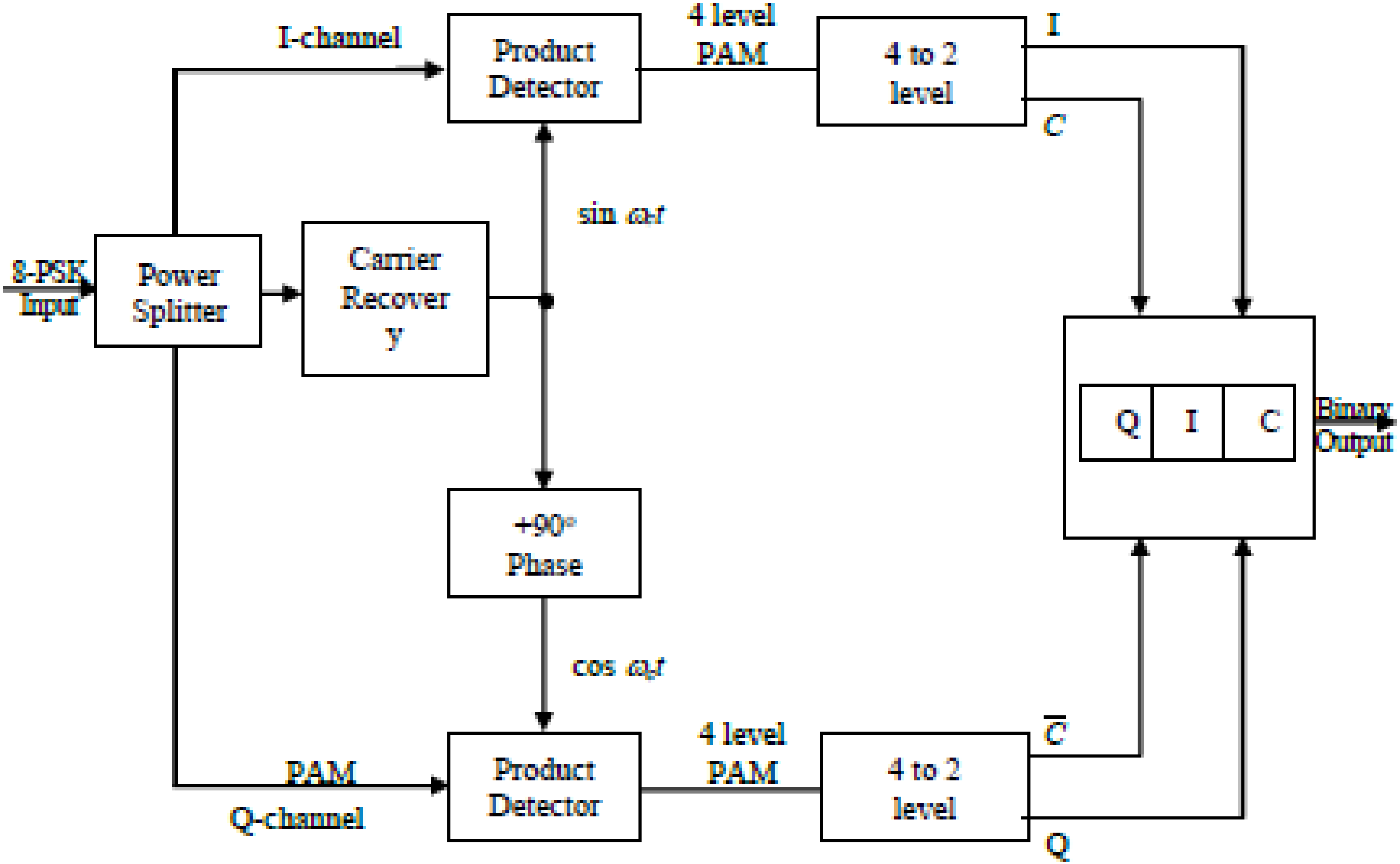
2-4 Levels Converter

I	C	Output
0	0	-0.541v
0	1	-1.307v
1	0	+0.541v
1	1	+1.307v

Q	$\bar{C}$	Output
0	1	-1.307v
0	0	-0.541v
1	1	+1.307v
1	0	+0.541v



8-PSK Receiver



Receiver of 8 PSK

- Power splitter directs the 8-PSK signal to the I and Q product detectors and carrier recovery circuit.
- Carrier recovery circuit reproduces the original reference oscillator signal.
- Incoming 8-PSK signal is multiplied with recovered carrier in I channel and quadrature carrier (after 90° phase shift) in Q channel.
- Outputs of product detectors (4 level PAM signal) are fed to 4-to-2 level analog-to-digital converters.
- Outputs from I channel 4-to-2 level converter are I and C bits while those from Q channel are Q and C.
- Parallel-to-serial logic circuit coverts I/C and Q/C bit pairs to serial I, Q, and C output data stream.

BW of 8 PSK

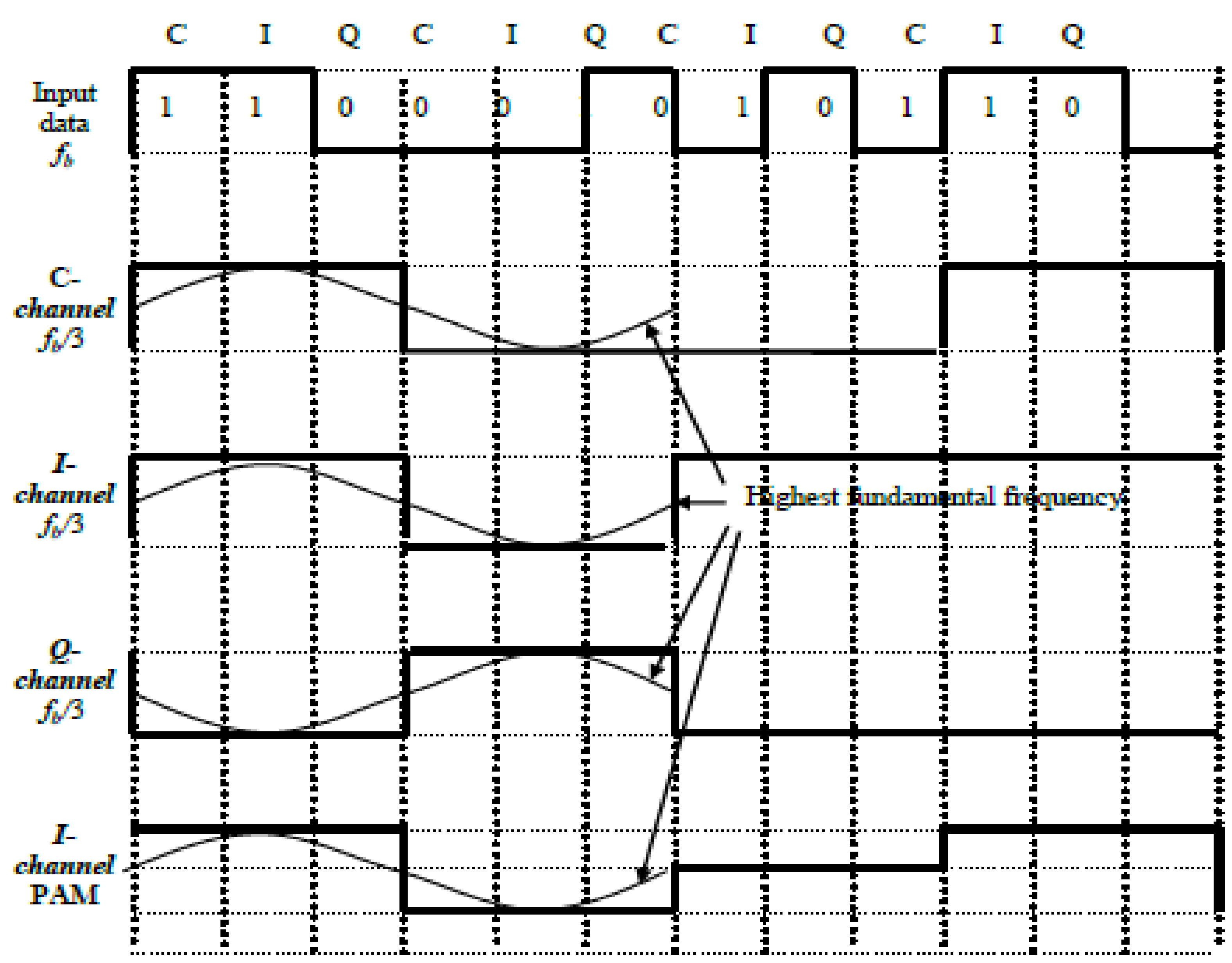
- Data are divided into three channels, bit rate in I, Q, or C is equal to 1/3 of input (i.e., $f_b/3$).
- Highest fundamental frequency in I, Q, or C channel is equal to 1/6 of input bit (i.e., $f_b/6$).
- Also highest frequency in either PAM is $f_b/6$ Balanced modulators output is the product of carrier and PAM signal:

$$Out = A \sin 2\pi f_a t \ \sin 2\pi f_c t = A \sin 2\pi \frac{f_b}{6} t \ \sin 2\pi f_c t$$

$$Out == \frac{A}{2}\left[\cos 2\pi\left(f_c - \frac{f_b}{6}\right) - \cos 2\pi\left(f_c + \frac{f_b}{6}\right)\right]$$

$$BW_{8\,PSK} = \left(f_c + \frac{f_b}{6}\right) - \left(f_c - \frac{f_b}{6}\right) = \frac{f_b}{3}$$

Highest Fundamental Frequency



16 PSK

16 PSK

- There are 16 different output phases possible.
- Modulator acts on the incoming data in groups of 4 bits (2^4=16), called quad bits.
- So, output phase does not change until 4 bits have been inputted into the modulator.
- Output baud rate and minimum bandwidth are equal to one-fourth of the incoming bit rate (fb/4).
- Angular separation between adjacent output phases is only 22.5°.
- Therefore, the signal can undergo almost a 11.25° phase shift during transmission
- So, 16-PSK is highly susceptible to phase impairments in the transmission medium.

QAM

Quadrature Amplitude Modulation

QAM

- QAM is a form of digital modulation, the information is contained in both the amplitude and the phase of the transmitted carrier.
- **8**-QAM is $\boldsymbol{M}$-ary encoding technique where $\boldsymbol{M} = 8$.
- **8**-QAM output is not a constant-amplitude signal such as **8**-PSK.
-

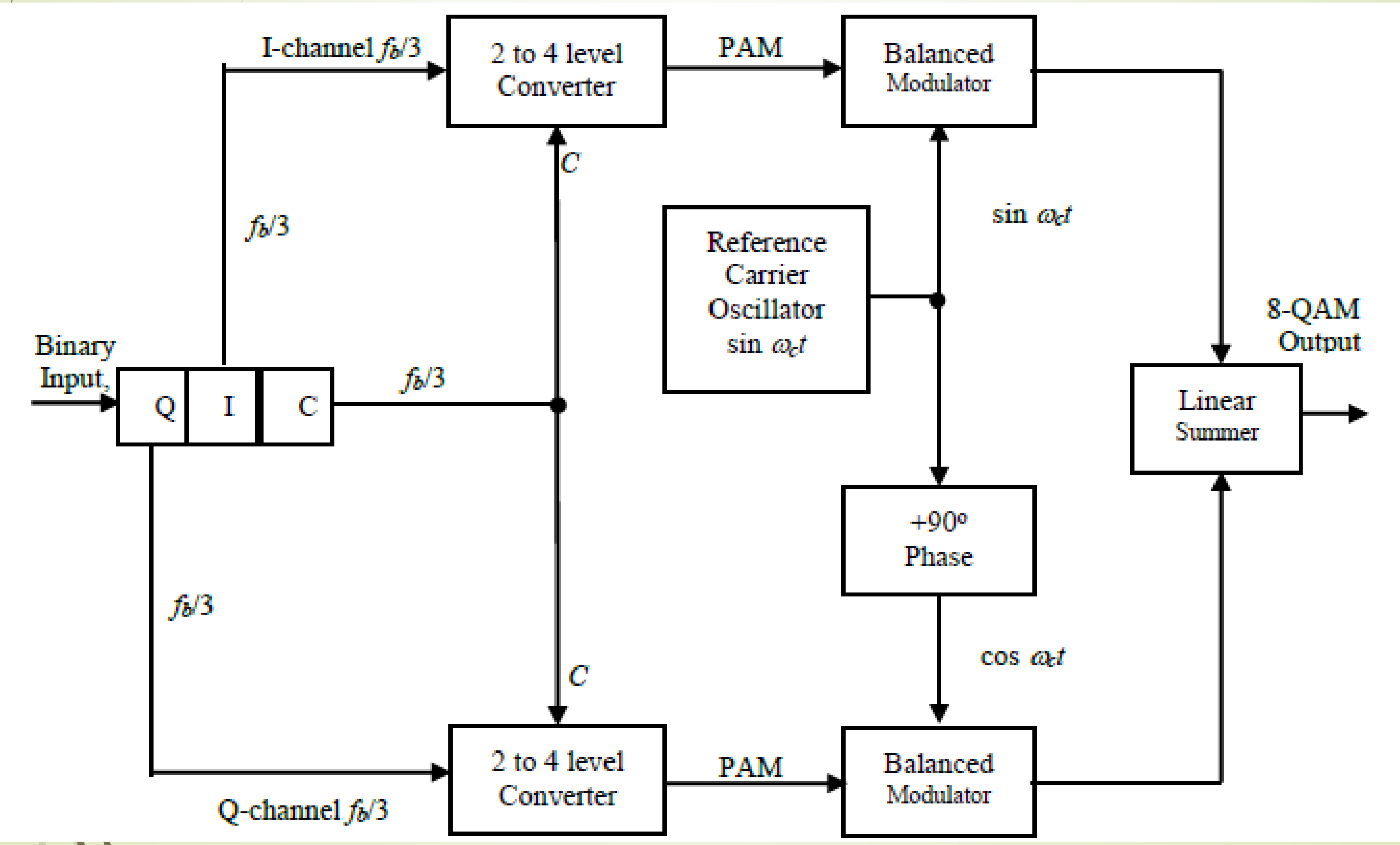
8-QAM Transmitter

- **8-QAM defers from 8-PSK in the inverter between the C and Q.**
- **Data are divided into I, Q, and C channels; each with a rate fb/3.**
- **I and Q bits determine the polarity of PAM signal at output of 2-to-4 level converters**
- **C channel determines the magnitude.**
- **8-QAM output is not a constant-amplitude signal such as 8-PSK.**

8-QAM Truth Table

BINARY INPUT			8-QAM OUTPUT	
Q	I	C	AMPLITUDE	PHASE
0	0	0	0.765 V	-135
0	0	1	1.848 V	-135
0	1	0	0.765 V	-45
0	1	1	1.848 V	-45
1	0	0	0.765 V	+135
1	0	1	1.848 V	+135
1	1	0	0.765 V	+45
1	1	1	1.848 V	+45

8-QAM Transmitter



Comparison

Table 2.2: Bandwidth Efficiency of Digital Modulation Techniques

Modulation	Encoding	Bandwidth, Hz	Baud rate	Efficiency, b/s/Hz
FSK	Single bit	$>f_b$	f_b	<1
BPSK	Single bit	f_b	f_b	1
QPSK	Di-bit	$f_b/2$	$f_b/2$	2
8-PSK	Tri-bit	$f_b/3$	$f_b/3$	3
8-QAM	Tri-bit	$f_b/3$	$f_b/3$	3
16-PSK	Quad-bit	$f_b/4$	$f_b/4$	4
16-QAM	Quad-bit	$f_b/4$	$f_b/4$	4

Carrier Recovery

Squaring Loop

- **The received BPSK signal is filtered to reduce the spectral width of noise.**
- **Squaring circuit**
  - **Removes the modulation and**
  - **Generates the second harmonic of carrier.**
- **This harmonic $2\omega_c$ is phase tracked by PLL.**
- **Frequency of PLL (VCO output) is then divided by 2 to be ω_c and used as a phase reference for the product modulators.**

BPSK Carrier Recovery

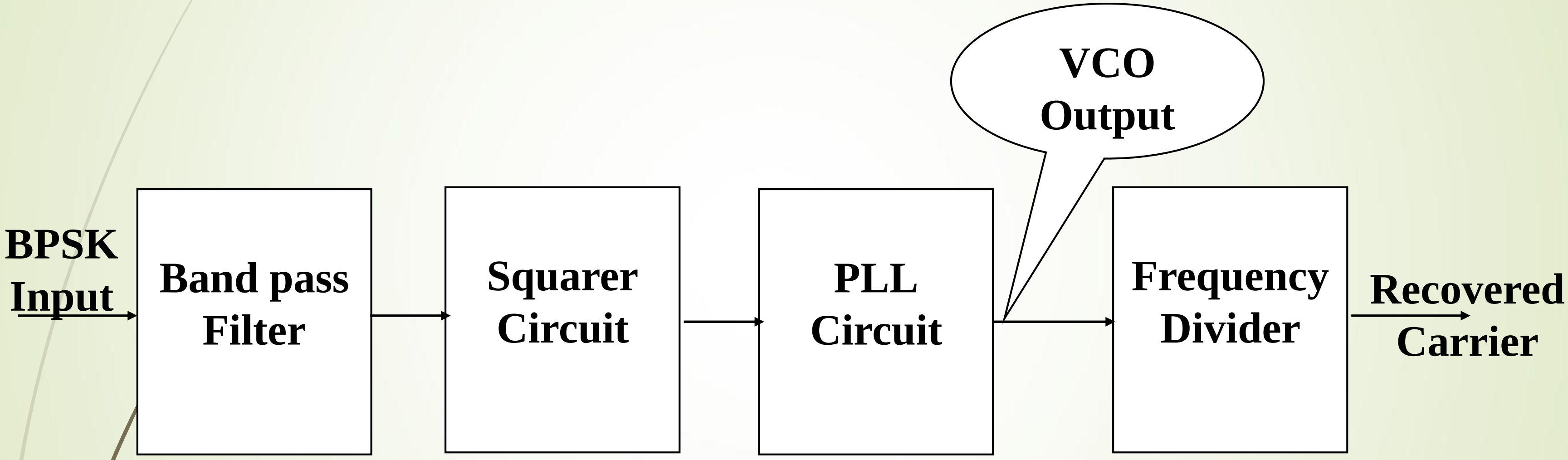


Fig.2.27 Squaring Loop Carrier Recovery for BPSK

Analysis of Squaring Loop

Assume receiving BPSK signal:

- **If received signal is $+\sin\omega_c t$, output of the squaring circuit is:**

$$Output = (+\sin\omega_c t)^2 = \frac{1}{2}[1 - \cos 2\omega_c t] \xRightarrow{Filtered} -\frac{1}{2}\cos 2\omega_c t$$

- **If received signal is $-\sin\omega_c t$, output of the squaring circuit is:**

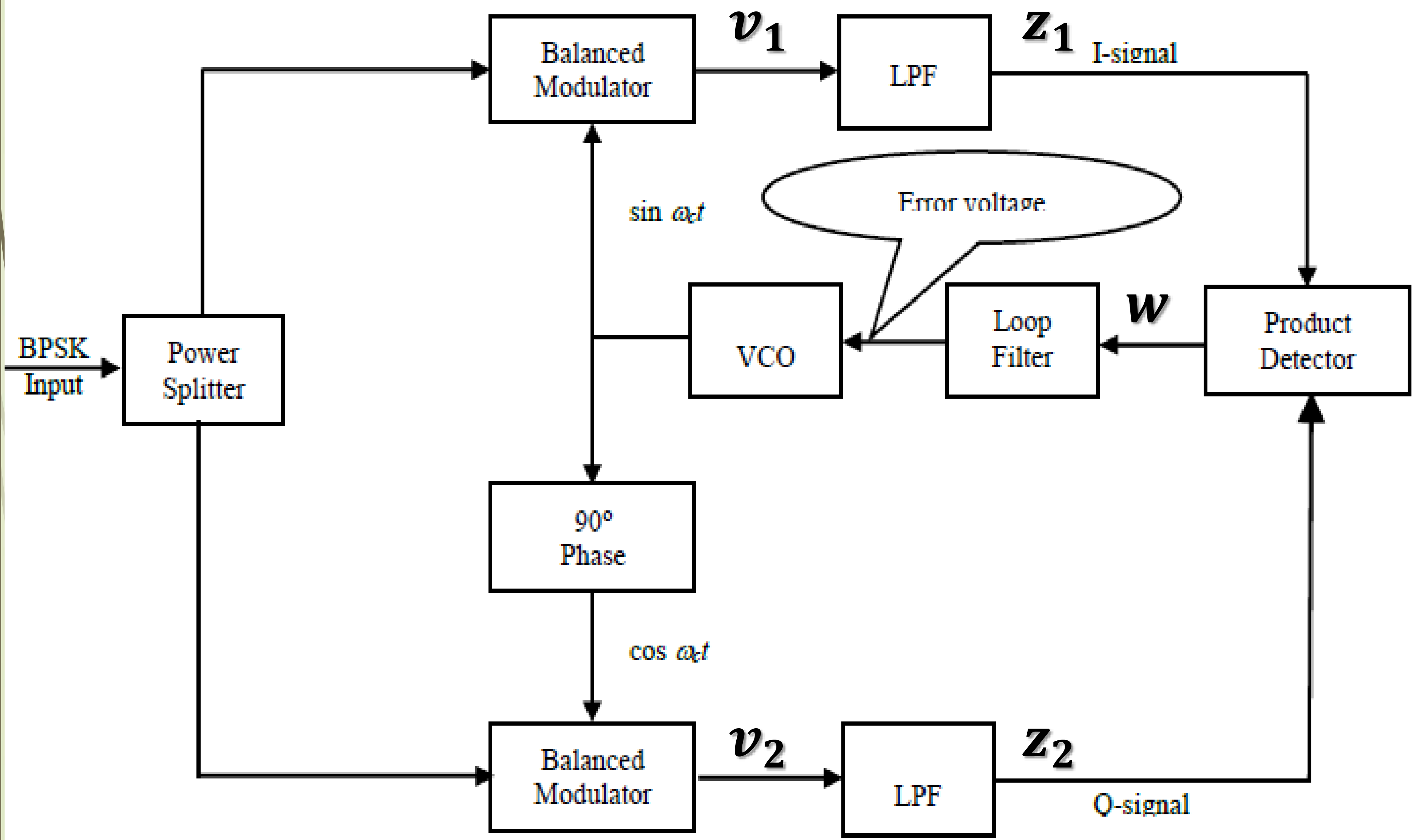
$$Output = (-\sin\omega_c t)^2 = \frac{1}{2}[1 - \cos 2\omega_c t] \xRightarrow{Filtered} -\frac{1}{2}\cos 2\omega_c t$$

- **The dc is removed by PLL filtering.**
- **PLL tracks the carrier phase.**
- **Finally, frequency divider return it to ω_c**

Costas Loop (Quadrature Loop)

- It uses two parallel tracking loops (I & Q)
  - To drive the product modulators
    - That drive the product detector
      - That drives the VCO.
- Product of I and Q signals will produce an error voltage proportional to phase error in VCO.
- This error voltage controls the phase and thus the frequency of the VCO.

Costas Loop Carrier Recovery



Analysis of Costas Loop

Assume the received signal: $r(t) = A\, m(t) \sin \omega_c t$

$$\therefore v_1(t) = [A\, m(t) \sin \omega_c t][\sin \omega_c t + \emptyset]$$

$$= \frac{A}{2} m(t)[\cos \emptyset - \cos(2\omega_c t + \emptyset)]$$

$$\therefore z_1(t) = \frac{A}{2} m(t) \cos \emptyset$$

$$\therefore v_2(t) = [A\, m(t) \sin \omega_c t][\cos \omega_c t + \emptyset]$$

$$= \frac{A}{2} m(t)[\sin \emptyset - \sin(2\omega_c t + \emptyset)]$$

$$\therefore z_2(t) = \frac{A}{2} m(t) \sin \emptyset$$

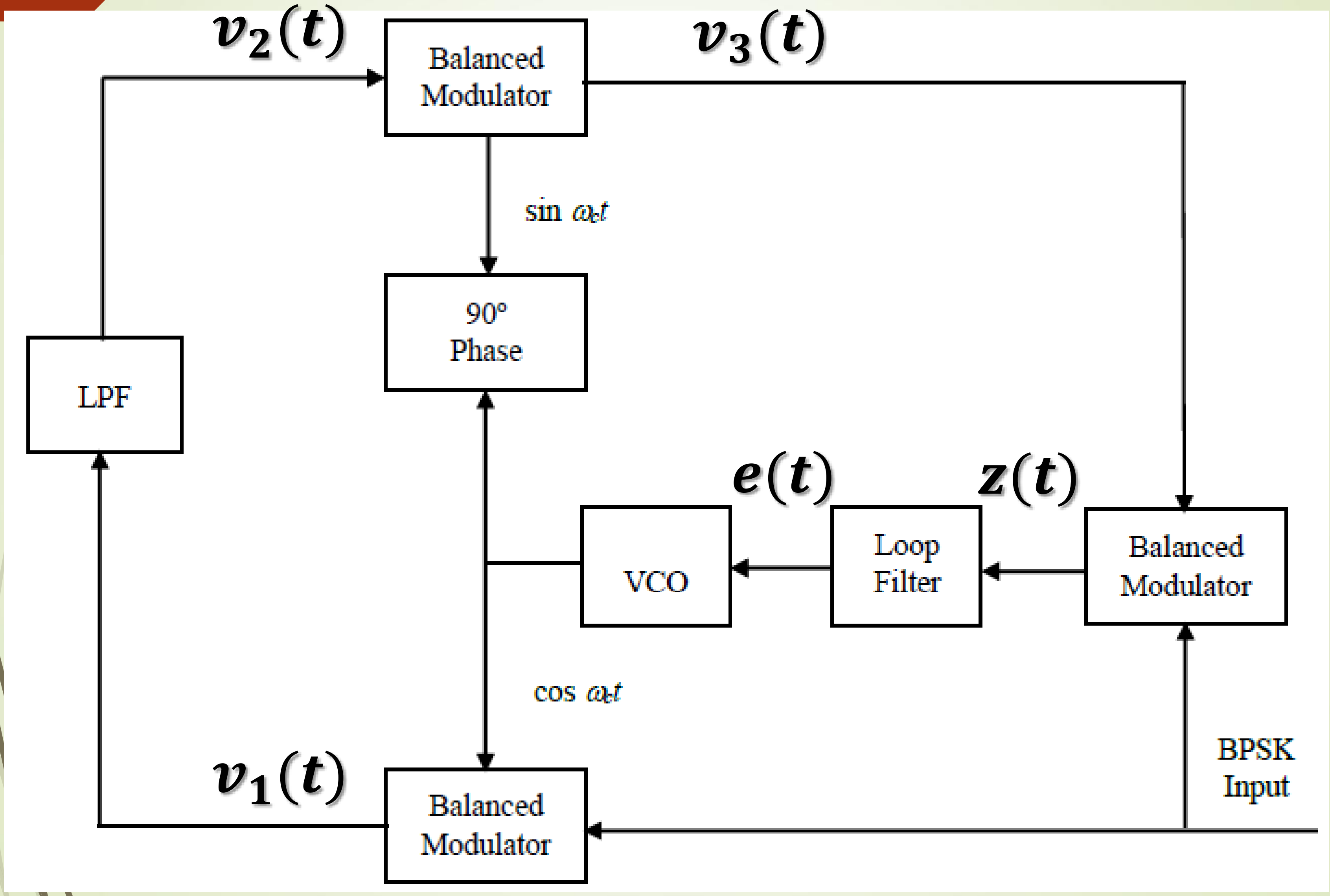
$$\therefore w(t) = z_1(t)\, z_2(t) = \frac{A^2}{4} m^2(t) \sin \emptyset \cos \emptyset$$

$$\therefore w(t) = \frac{A^2}{4} m^2(t) \sin 2\emptyset$$

Re-modulator Loop

- **Re-modulator produces a loop error voltage that is proportional to twice the phase error between the incoming signal and the VCO signal.**
- **So, it has a faster acquisition time than squaring loop**

Re-modulator Loop Carrier Recovery



Analysis of Re-modulator

Assume the received signal: $r(t) = A\,m(t)\sin\omega_c t$

$$\therefore v_1(t) = [A\,m(t)\sin\omega_c t][\cos\omega_c t + \emptyset]$$

$$= \frac{A}{2}m(t)[\sin\emptyset - \sin(2\omega_c t + \emptyset)]$$

$$\therefore v_2(t) = \frac{A}{2}m(t)\sin\emptyset$$

$$\therefore v_3(t) = \left[\frac{A}{2}m(t)\sin\emptyset\right][\sin\omega_c t + \emptyset]$$

$$= \frac{A}{4}m(t)\cos\omega_c t - \frac{A}{4}m(t)\cos(\omega_c t + 2\emptyset)$$

$$\therefore z(t) = \left[\frac{A}{4}m(t)\cos\omega_c t - \frac{A}{4}m(t)\cos(\omega_c t + 2\emptyset)\right]A\,m(t)\sin\omega_c t$$

$$\therefore z(t) = \frac{A^2}{8}m^2(t)\sin 2\omega_c t - \frac{A^2}{8}m^2(t)[\sin 2\emptyset + \sin(2\omega_c t + 2\emptyset)]$$

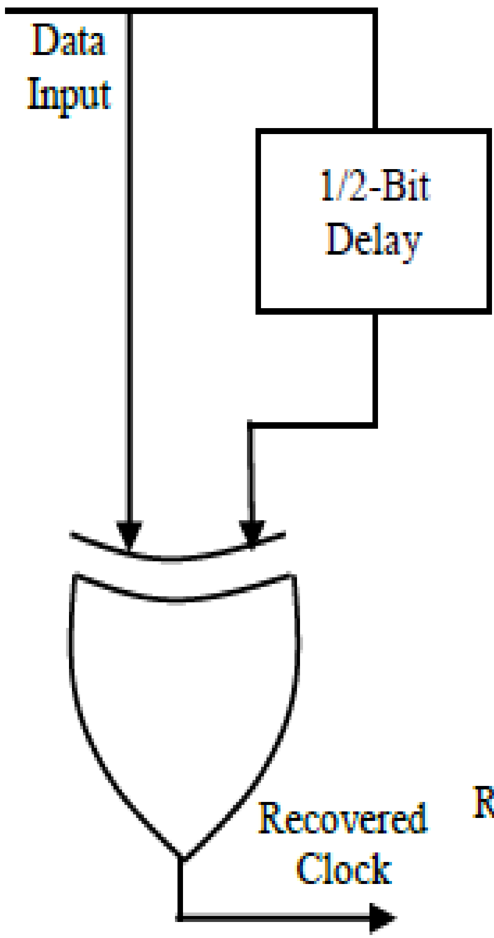
$$\therefore e(t) = -\frac{A^2}{8}m^2(t)\sin 2\emptyset$$

Clock Recovery

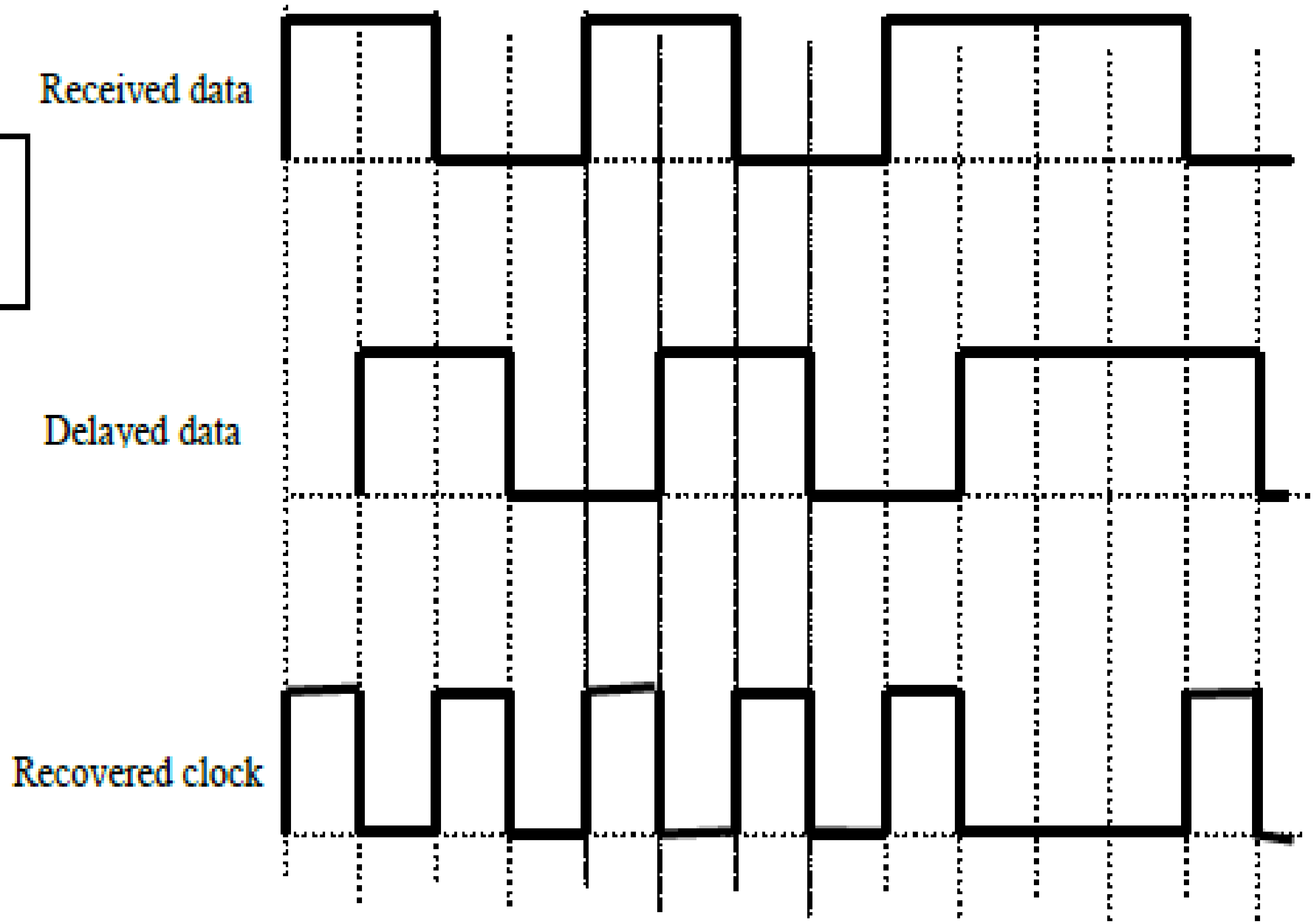
Clock Recovery

- Digital radio requires precise timing or clock synchronization between transmit and receive circuitry.
- Simple circuit used to recover clocking information from the received data.
- Data is delayed by **one-half** a bit time and compared with the original data in an **XOR**.
- Frequency of clock that is recovered with this method is equal to received data rate f_b.
- However, if received data has period of successive 1's or 0's, received clock is lost.

Simple Clock Recovery Circuit



(a) Circuit diagram



(b) Timing diagram

Differential PSK

Differential PSK

- In DPSK is the information is contained in the difference between two successive phases rather than the absolute phase.
- So, it is not necessary to recover a phase coherent carrier.
- Instead, a received data is delayed by one time slot and then compared to the next received bit

DBPSK Modulator

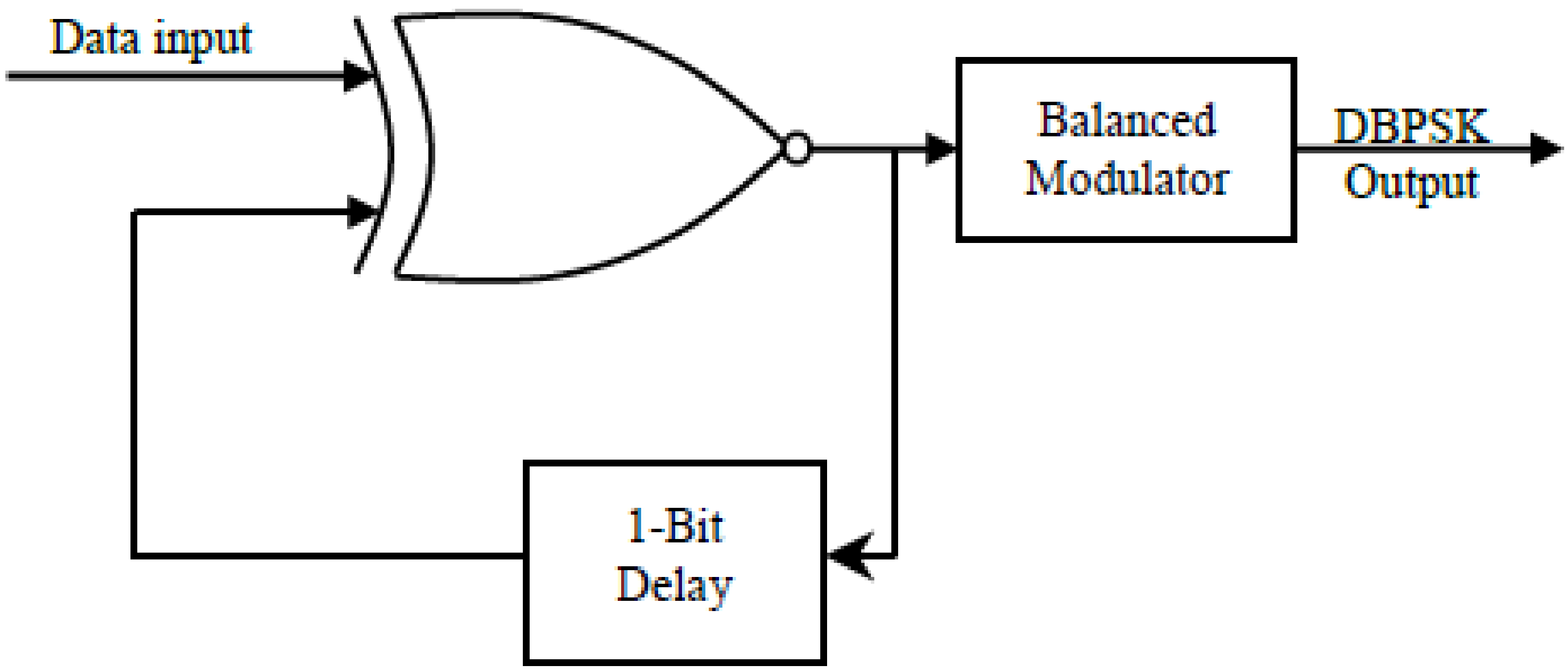


Fig.3.31 DBPSK Modulator

Transmitter of DBPSK

- Incoming information bit is XNORed with the preceding bit prior to the modulator;
  - If they are the same, the XNOR output is a logic 1;
  - If they are different, it will be logic 0.
- An initial reference bit is assumed.
- Figure shows relationship between:
  - input data,
  - XNOR output and
  - phase of modulator output.

Operation of DBPSK

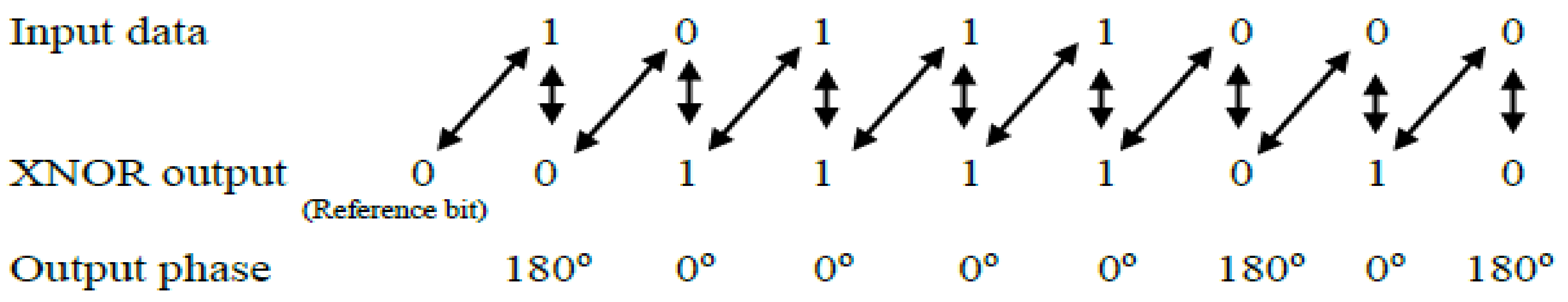


Fig.3.32: Timing Diagram of BDPSK Transmitter

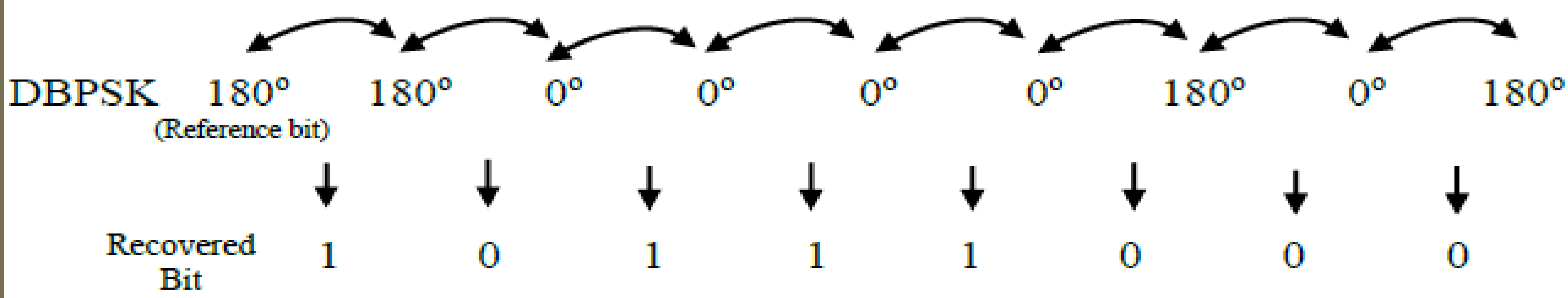


Fig.2.3:4 Timing Diagram of BDPSK Receiver

Receiver of DBPSK

- Received signal is delayed by one bit time,
- Then compared with the next bit in the balanced modulator.
  - If they has the same phase, +V is generated (logic 1), or
  - Otherwise –V is generated (logic 0)
- The timing sequence is shown

Demodulation of DBPSK

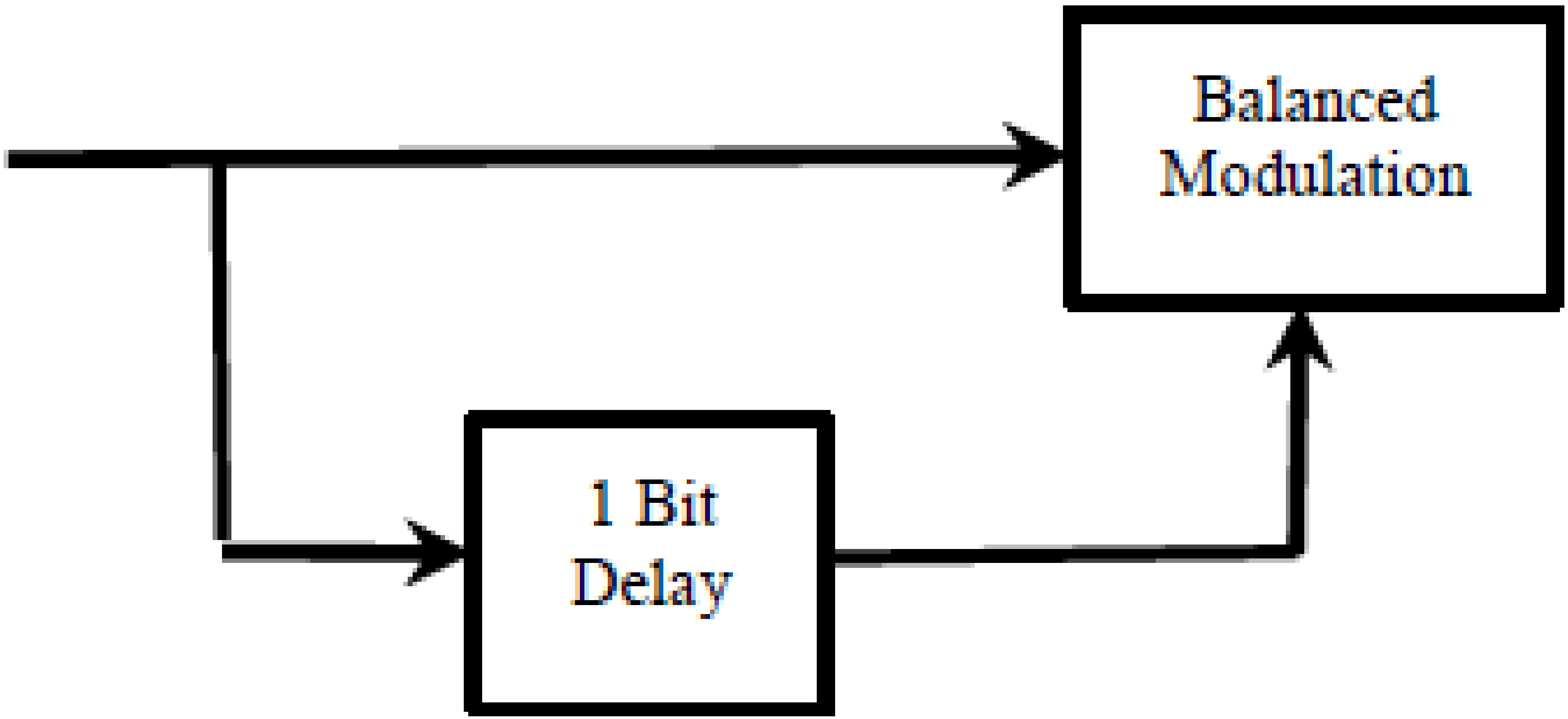


Fig.2.33 DBPSK Demodulator

Probability of Error

Probability of Error & BER

- Probability of error P_e is a theoretical expectation of the bit error rate BER for a given system.
- BER is an empirical (or historical) record of the system's actual bit error performance.
- However, practically:
  - P_e referred to symbol error rate
  - BER is the bit error rate

Probability of Error P_e

- Probability of error P_e depends on
  - Carrier-to-noise ratio.
    - Or average energy per bit-to-noise power density ratio.
  - No of possible encoding conditions.

Thermal Noise, *N*

- ***N*** **is expressed in terms of Boltzmann constant ($K=1.38\times10^{-23}$ J/K), room temperature ($T=290^{o}K$), and system bandwidth B in Hz as:**

$$N = KTB \quad (watts)$$

$$N = 10\,Log\,\frac{KTB}{0.001} \quad (dBm)$$

dbm **means the power to mill watts.**

100 Carrier to Noise Ratio C/N

$$\frac{C}{N} = \frac{C(watts)}{KTB(watts)} \quad (dimensionless)$$

$$\frac{C}{N} = 10Log\left(\frac{C}{KTB}\right) \quad (dB)$$

$$\frac{C}{N} = C(dBm) - N(dBm)$$

Bit Signal to Noise Ratio E_b/N_o

- Energy per bit-to-noise power density ratio Eb/No is the ratio of
  - Energy of a single bit E_b to
  - Noise power present in 1 Hz of BW, N_o.
- It is used to compare all digital modulation systems that use different:
  - Transmission rates (bps),
  - Modulation techniques (e.g., PSK, FSK, MSK, OOK, …)
  - Encoding techniques (e.g., QPSK, 8-PSK, 16-PSK, …).
- So it normalizes all multiphase schemes to a common noise bandwidth allowing for simple and more accurate comparison of their error performance.

Average energy per bit E_b

- Average energy per bit Eb is related to the carrier power C and the bit duration Tb as:

$$E_b = C\,T_b = \frac{C}{f_b}, \qquad (Joul)$$

$$E_b = 10\,Log\left(\frac{C}{f_b}\right) = 10\ \mathrm{Log\ C} - 10\ \mathrm{Log}\ f_b \quad (dB)$$

Average Noise Spectral Density N_o

- **Noise power density N_o is the thermal noise power normalized to a 1 Hz bandwidth:**

$$N_o = \frac{N}{B}, \qquad (watts/Hz)$$

$$E_b = 10\ Log\left(\frac{C}{f_b}\right) = 10\ \mathrm{Log\ C} - 10\ \mathrm{Log}\ f_b \quad (dB)$$

E_b/N_o

$$\frac{E_b}{N_0} = \frac{C/f_b}{N/B} = \frac{CB}{Nf_b}$$

$$\frac{E_b}{N_0} = 10\ Log\ E_b - 10\ Log\ N_o \quad (dB)$$